



LTE Cat-M1 / IoT Antenna Specifications



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LSP69001299

FEATURES

- LTE Cat-M1/NB-IoT
- Quicker time to market
- Standard Product
- Smaller Form Factor & Ground Clearance Requirements

ADVANTAGES

- Eliminates External antennas
- Fewer design changes. Simple implementation
- Speeds development time and reduces costs since reduces NRE and custom development time
- Can be used in a variety of custom form factors and applications



DESIGN GUIDELINES

INTRODUCTION

The LSP69001299TR LTE NB-IoT Antenna can be designed into many wireless product types using small form factor board. The following sections explain KYOCERA AVX' recommended layouts to help the designer integrate the antennas into a product with optimum performance.

ELECTRICAL SPECIFICATIONS

Typical performance antenna measured on 60 x 40 mm PCB

Frequency (MHz)	On 60x40 mm PCB			
	B12	B13	B20	1710 - 2170
Return Loss	<-2.5 dB			<-3 dB
Efficiency	15 %			42 %
Peak Gain	-2.4 dBi @ 740 MHz	-2.8 dBi @ 750 MHz	-3.0 dBi @ 815 MHz	1.3 dBi @ 2030 MHz
Impeadance	50 ohms unbalanced			

MECHANICAL SPECIFICATIONS

Ordering Part Numbers	LSP69001299TR
Dimensions (mm)	35.00 ± 0.10 length 9.00 ± 0.10 width 3.20 ± 0.10 thickness
Mechanical mounting	SMT (P&P)
Weight (grams)	0.2 grams
Color	Black

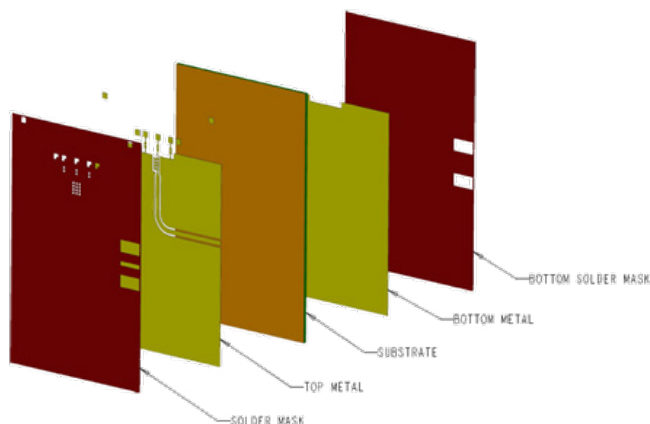
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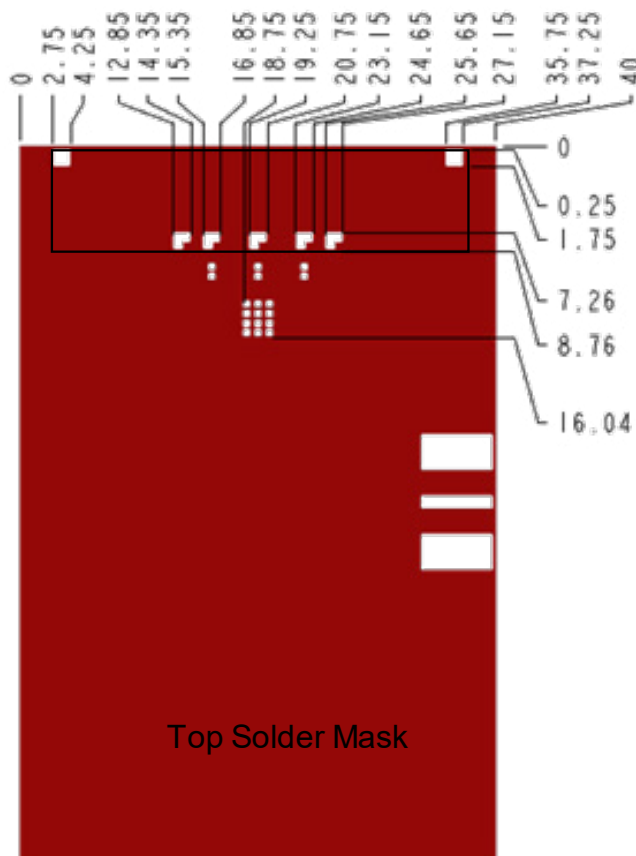
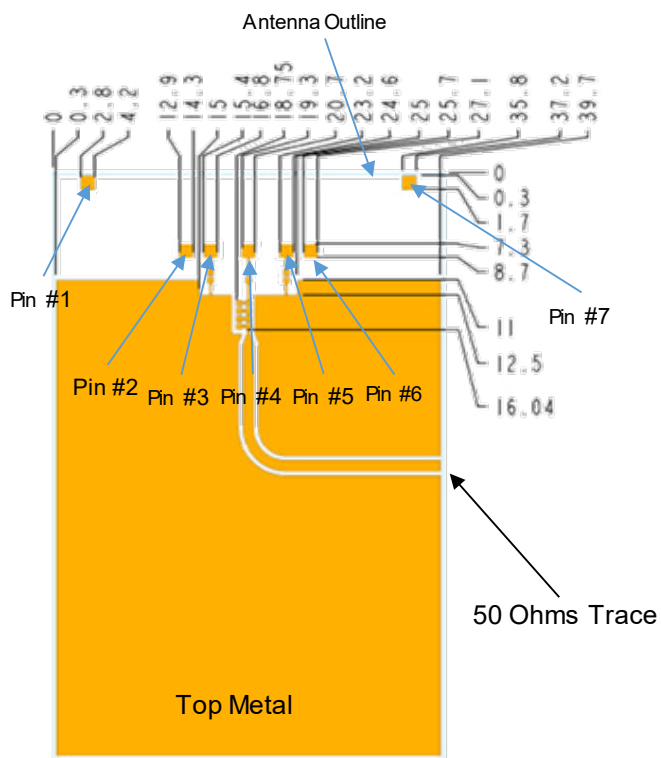
FEATURES

Typical layout dimensions in mm

Pin#	Description
1	Dummy Pad
2	Dummy Pad
3	Ground
4	Feed
5	Ground
6	Dummy Pad
7	Dummy Pad



- Additional vias : Diam. 0.2 mm to be placed around antenna, (no vias on transmission lines)

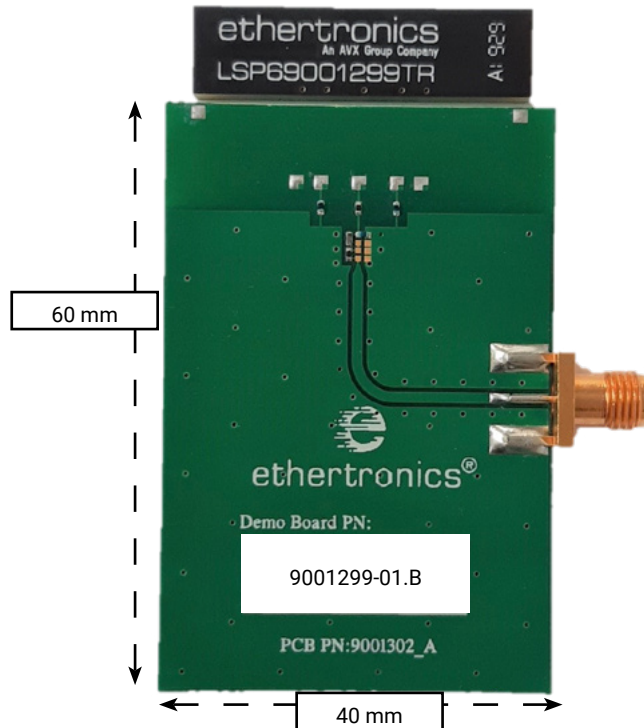


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ANTENNA LOCATION

The Figure below shows LSP69001299TR typical landing location of LTE Cat-M1/NB-IoT Antenna



ANTENNA TUNING GUIDELINES

The board size and antenna location are the most important factor for antenna performance. The smaller the board size, the lower the low band performance will be. Nonetheless, antenna performance can be improved by optimizing the matching components.

Here are some studies to help identifying the optimum circuit matching and the best battery position far from antenna:

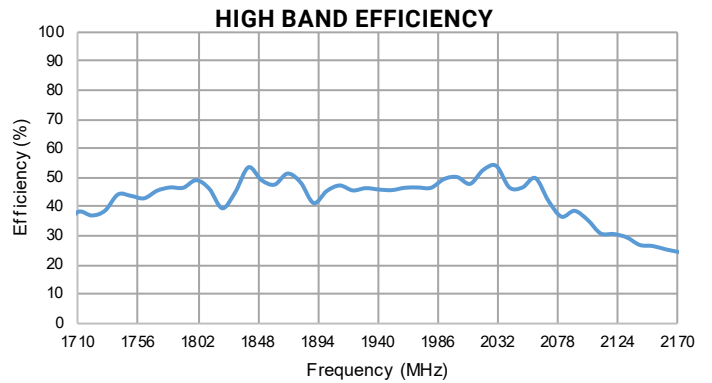
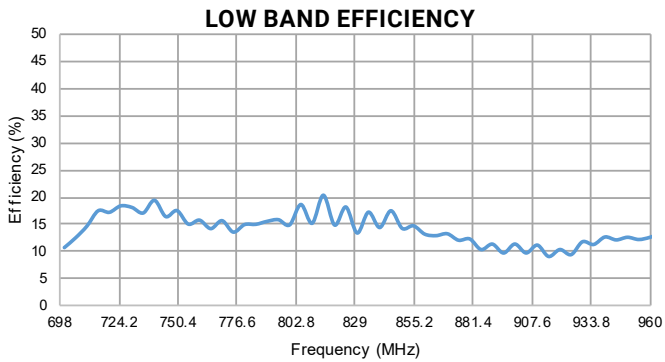
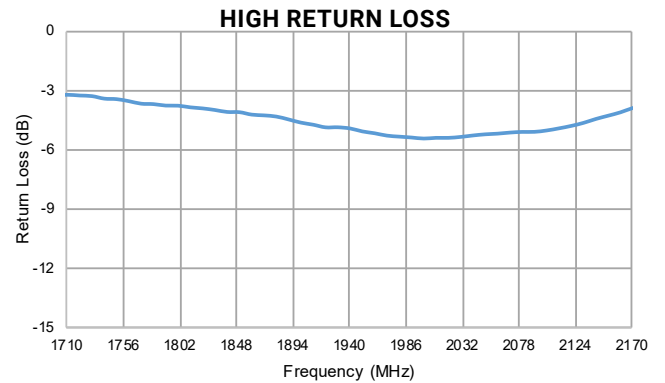
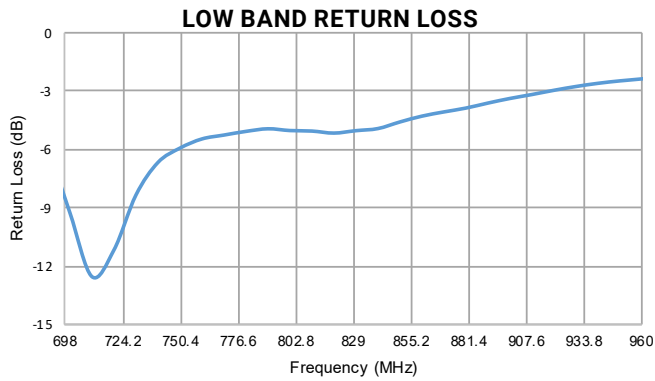
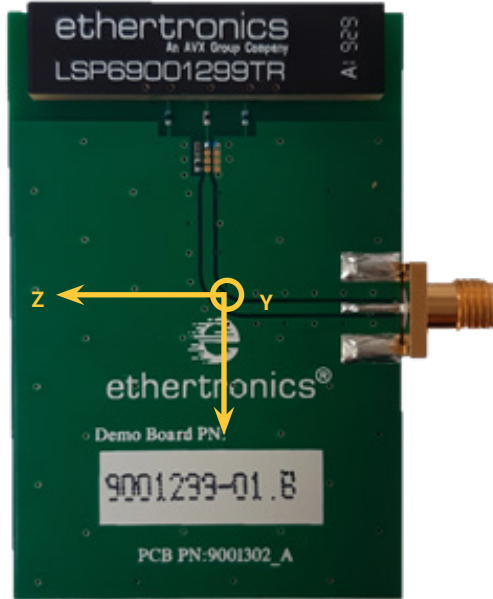
- Study 1: Antenna performance using the circuit matching
- Study 2: Antenna performance variation based on R1 and R2 effect
- Study 3: Antenna performance variation based on S1 effect
- Study 4: Antenna performance variation with different battery position

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RETURN LOSS AND EFFICIENCY PLOTS

Typical Performance measured with 60 x 40 mm PCB

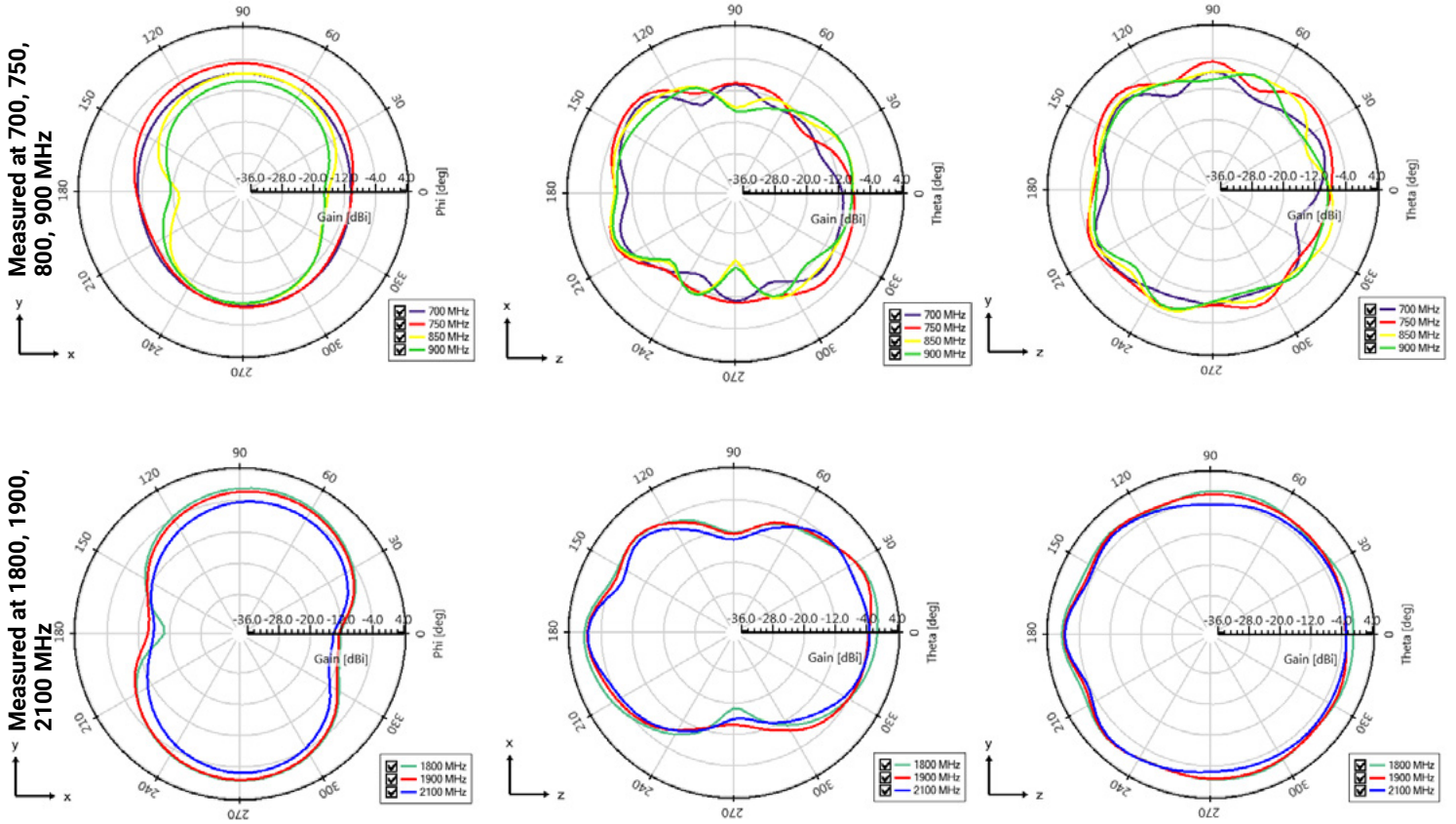
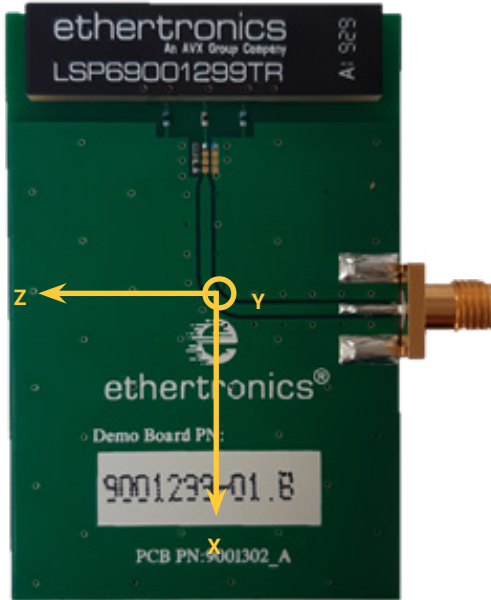


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RADIATION PATTERN PLOTS

Typical performance measured with 60 x 40 mm PCB
 Measured at 700, 750, 850, 900, 1800, 1900, 2100 MHz

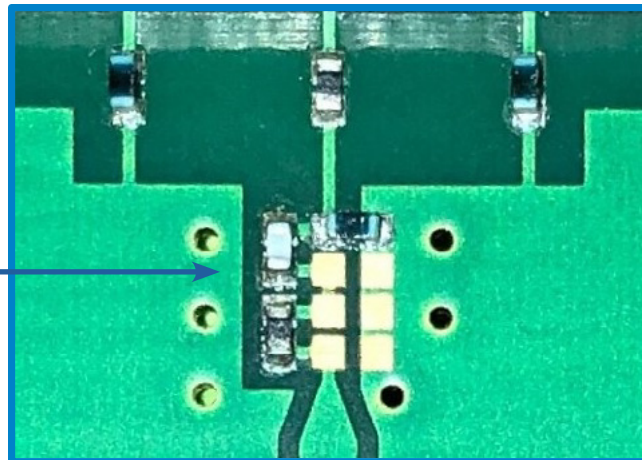
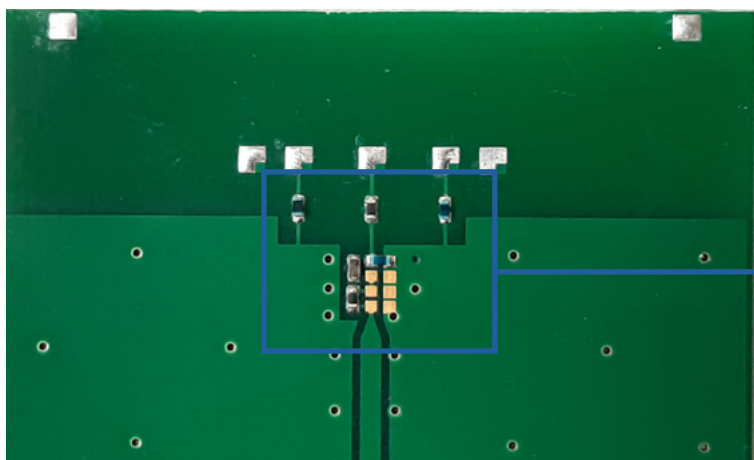


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ANTENNA MATCHING NETWORK (LSP69001299TR)

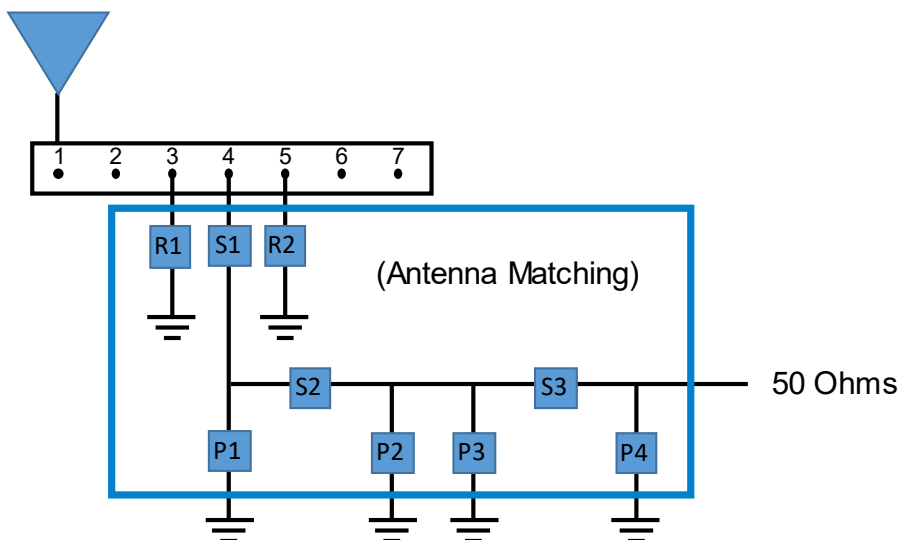
Typical matching values on 60 x 40 mm PCB



Antenna Matching

(Antenna Matching): pads are directly in line with

Pin#	Description
1	Dummy Pad
2	Dummy Pad
3	Ground
4	Feed
5	Ground
6	Dummy Pad
7	Dummy Pad



ANTENNA MATCHING CIRCUIT

	S1/S3	S2	P1	P2/P3/P4	R1	R2
Defaulting Matching	0 Ohm	2pF	13nH	DNI	20nH	22nH

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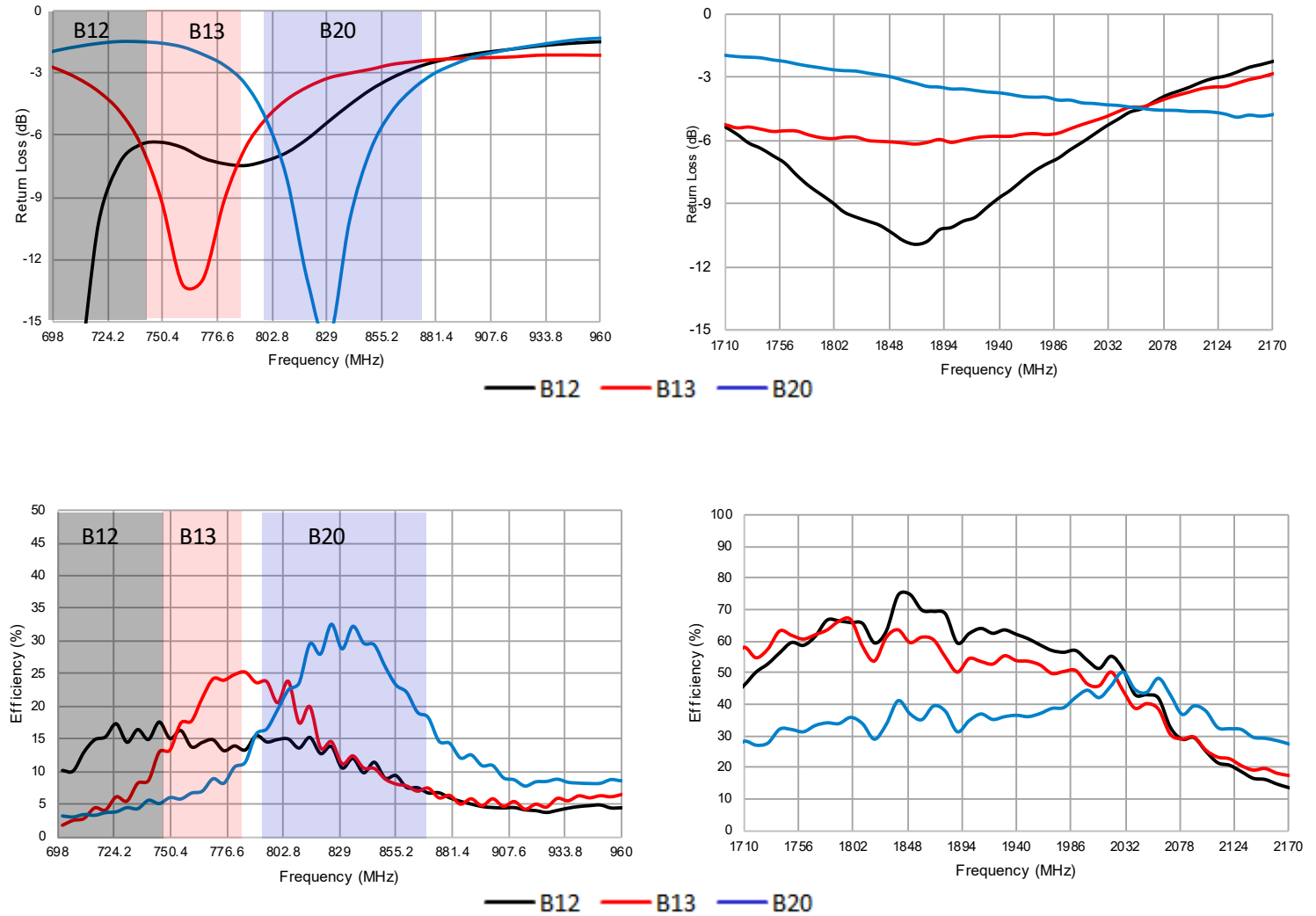
STUDY 1: ANTENNA MATCHING NETWORK FOR B12, B13 AND B20

Measured on 60 x 40 mm PCB

	S1/S3	S2	P1	P2	P3/P4	R1	R2
B12 Matching	0 Ohm	2.6pF	8.2nH	8.2nH	DNI	22nH	22nH
B13 Matching	0 Ohm	3.5pF	10nH	DNI	DNI	18nH	18nH
B20 Matching	0 Ohm	1.5pF	22nH	DNI	DNI	18nH	18nH

RETURN LOSS AND EFFICIENCY PLOTS

Below are typical performances using Ethertornics Standard demo-board.



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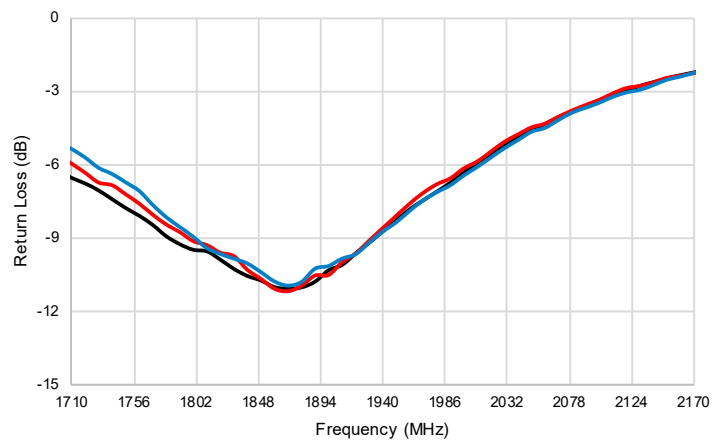
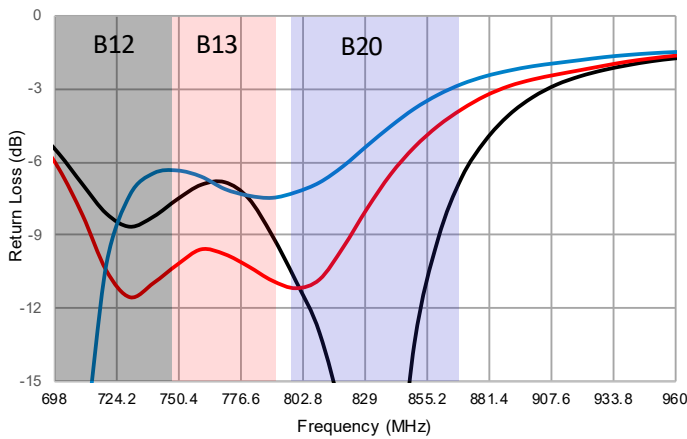
STUDY 2: ANTENNA MATCHING NETWORK / THE R1 AND R2 EFFECT ON THE LOW BAND PERFORMANCE

Measured on 60 x 40 mm PCB

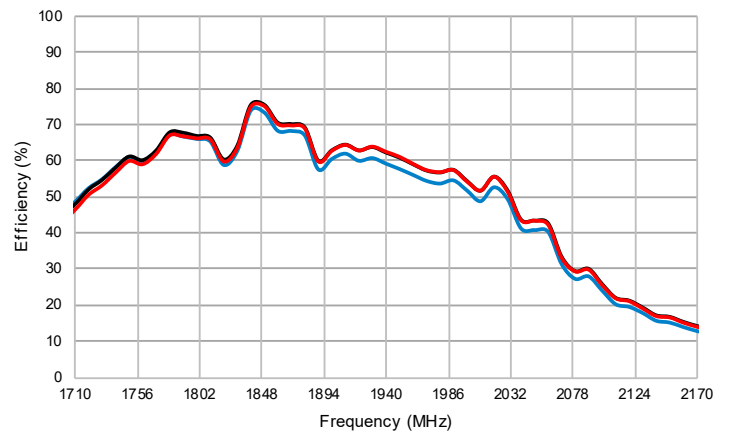
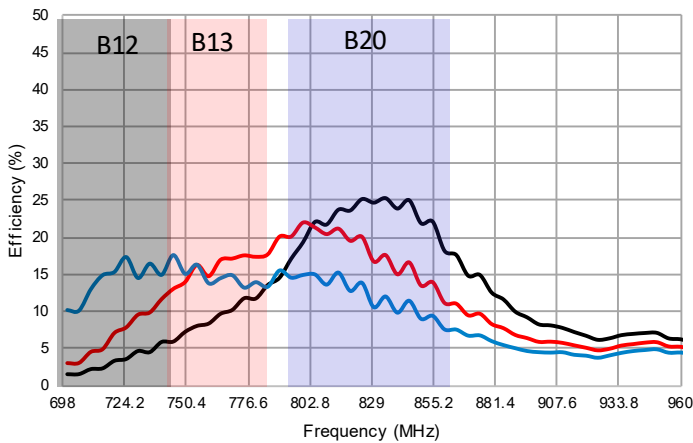
	S1/S3	S2	P1	P2	P3/P4	R1	R2
Config1	0 Ohm	2.6pF	8.2nH	8.2nH	DNI	15nH	15nH
Config2	0 Ohm	2.6pF	8.2nH	8.2nH	DNI	18nH	18nH
Config3	0 Ohm	2.6pF	8.2nH	8.2nH	DNI	22nH	22nH

RETURN LOSS AND EFFICIENCY PLOTS

Measured on 60 x 40 mm PCB



— Config1 — Config2 — Config3



— Config1 — Config2 — Config3

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STUDY 3: ANT ENNA MATCHING NETWORK / THE EFFECT OF S1 ON THE HIGH BAND PERFORMANCE

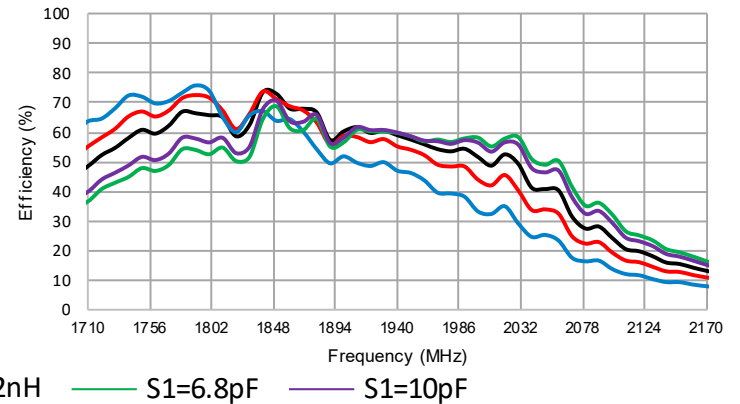
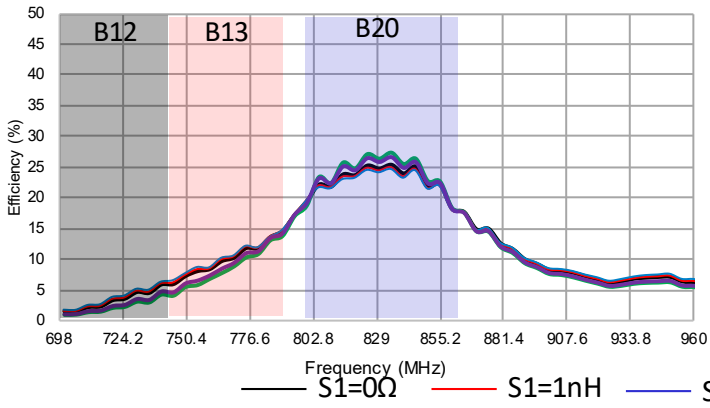
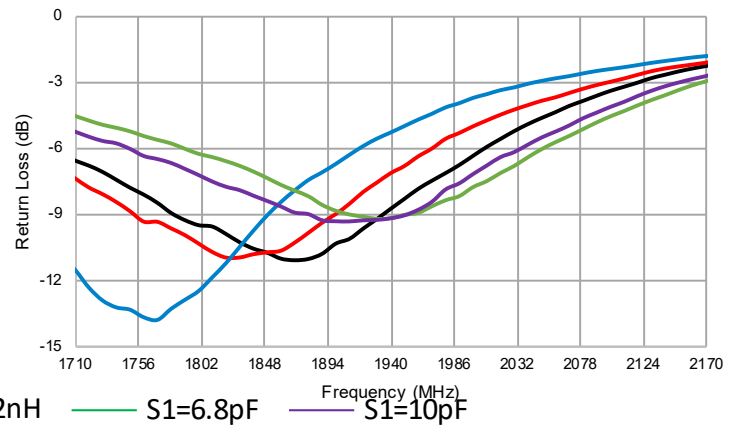
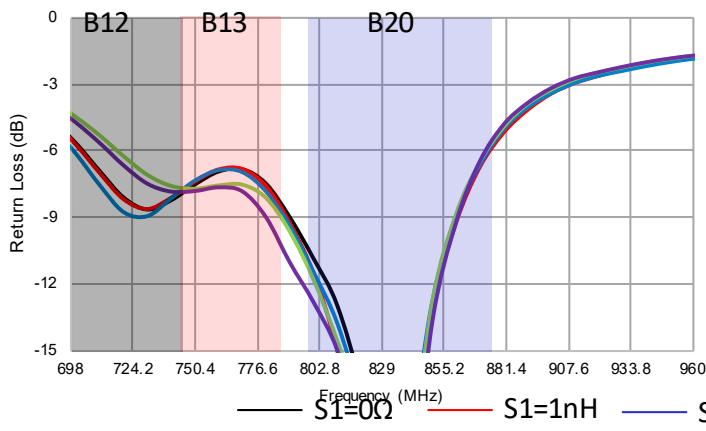
Measured on 60 x 40 mm PCB

	S3	S2	P1	P2	P3/P4	R1	R2
Config1	0 Ohm	2.6pF	8.2nH	8.2nH	DNI	15nH	15nH

	Config1	Config A	Config B	Config C	Config D
S1	0 Ohm	1nH	2nH	6.8pF	10pF

RETURN LOSS PLOT AND EFFICIENCY PLOTS

Measured on 60 x 40 mm PCB

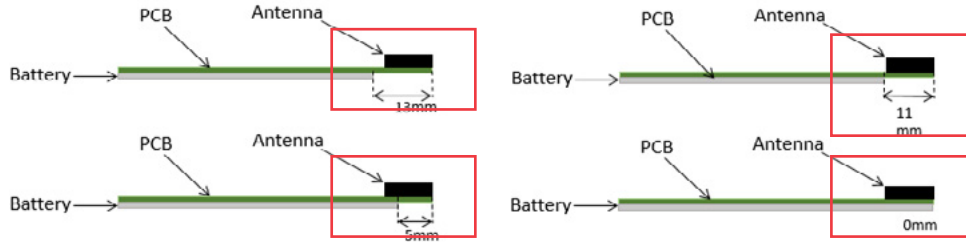


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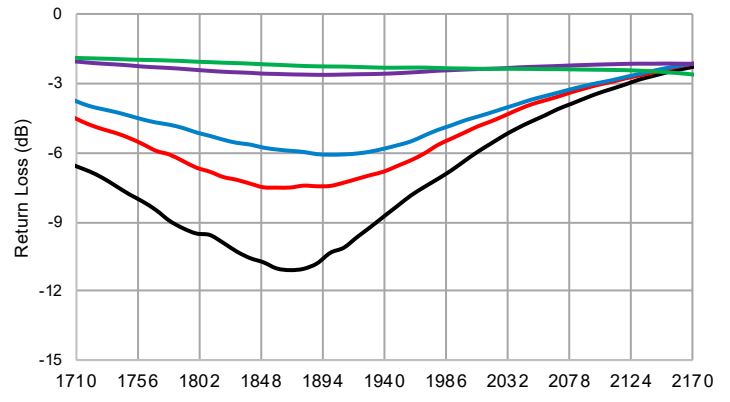
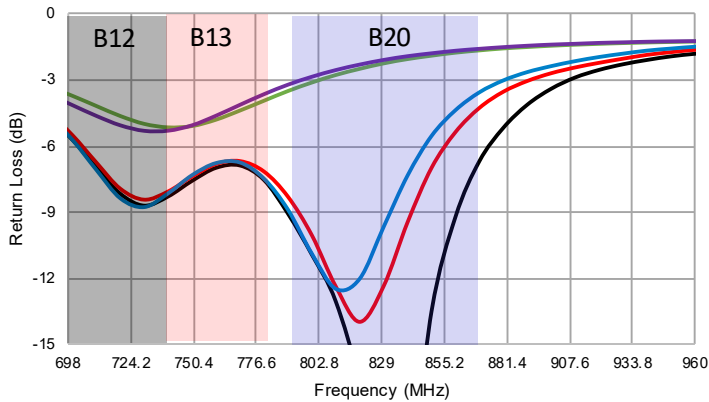
STUDY 4: THE BATTERY POSITION EFFECT UNDER THE EVB

Measured on 60 x 40 mm PCB with matching Config1

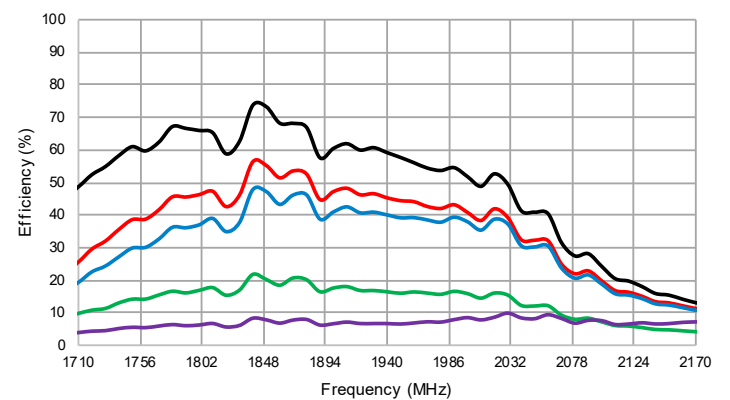
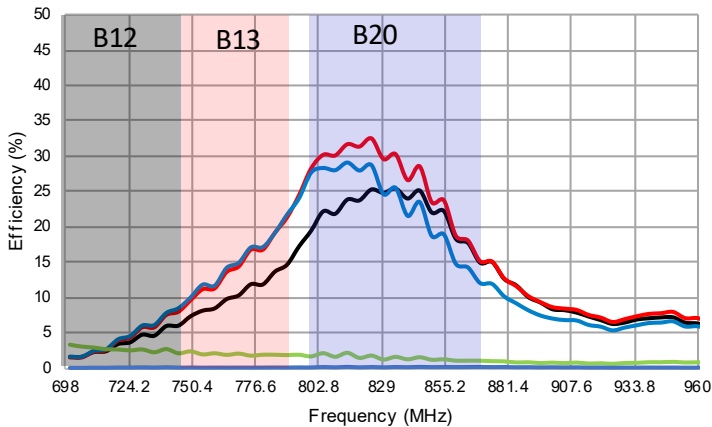


BATTERY POSITION EFFECT: RETURN LOSS AND EFFICIENCY PLOT (LSP69001299TR WITH MATCHING CONFIG1)

Measured on 60 x 40 mm PCB



— W/o battery — 13mm — 11mm — 5mm — 0mm



— W/o battery — 13mm — 11mm — 5mm — 0mm


PASTE STENCIL RECOMMENDATION

The same page as in P822601 application note page 22



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