



# Differential Clock Oscillator

## F SERIES

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### BASIC OVERVIEW

Clock Oscillator has realized excellent jitter performance and lower current consumption based on non-PLL oscillation circuit.

Also, the clock oscillator contributes to not only higher-speed data transmission, but also to power energy efficiency.

### KEY SPECIFICATIONS

Low Phase Jitter

Low Current Consumptions

Miniature Package Size Available:  
2016/2520/3225

### GENERAL CHARACTERISTICS

Frequency Tolerance: +/-50ppm

Temperature Range:

-40~85deg., -40~105deg., -40~125deg.

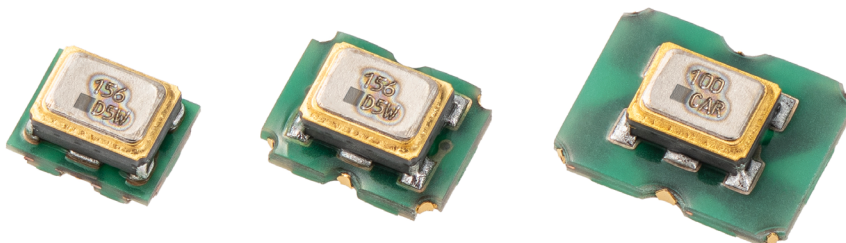
Output: HCSSL, LV-PECL, LVDS

### APPLICATIONS

- AI Server
- Data Center
- Network
- ADAS
- Optical Module

### ADVANTAGES VS. OUR COMPETITOR'S PRODUCTS

- Strong financial position through stable management
- Low phase noise products
- Unique technology and collaboration with IC manufacturers





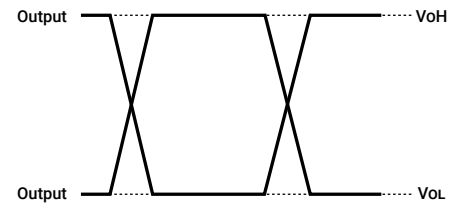
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### TOP SELLING POINTS / CHARACTERISTICS

- Excellent Jitter Performance: 40fs typ.
- Low Current Consumption: 20mA typ.
- Can Satisfy Automotive Quality “AEC-Q100/200 Compliant”
- Miniature Package Size Available: 2016/2520/3225



### FAQ'S

#### Q: How long is the lead time?

A: 18 week.

#### Q: What is “phase jitter”?

A: Phase jitter is the variation in the timing of a clock signal's edges from their ideal positions.

#### Q: What is the output difference between LV-PECL, LVDS and HCSL?

A: LV-PECL makes it possible to transmit signals over long-distances. LVDS has stable edges for high-speed communication, which contributes to ADAS and other applications. HCSL is optimized for short-distance, high-frequency applications.

#### Q: What is the advantage of differential clock oscillator in comparison with CMOS?

A: Differential clock oscillator has advantage of excellent jitter performance, noise resistance, higher-speed data transmission, etc.

*\*Noise resistance: the ability to keep signals stable by preventing disturbance from external noise*



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