TECHNICAL PAPER

Reliability and Characterization of MLCC Decoupling Capacitors With C4 Interconnections

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Abstract

Multilayer ceramic (MLC) capacitors are composite structures made of alternating layers of ceramic (dielectric material) and metal (electrodes). The dielectric material is barium titanate-based ceramic and the electrodes are made of platinum. C4 (controlled collapse chip connections) technology [1] is used to provide multiple attachment points to substrates. A high dielectric constant of barium titanate-based ceramic helps to achieve a large capacitance/size ratio. The capacitance ranges from 32 nF to 100 nF in body sizes up to 1.85 x 1.6 x 0.85 mm. In this paper, we cover design, reliability and electrical characterization of capacitors with C4 interconnections. Reliability stress tests performed during qualification were designed to cover a wide range of field applications and included stress tests such as liquid to liquid thermal shock, moisture resistance and thermal cycles per Mil. Std., high temperature bias, temperature humidity bias and tensile pull. A visual inspection of parts post stress and physical analysis of unstressed parts were also performed. The parameters monitored during stress testing were: capacitance, leakage current and plate resistance. The electrical characterization measurements included effects of frequency, temperature and voltage. Inductance measurements were included based on a self-resonance technique.

KYOCERA AVX

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1. Introduction

Over the last two years two new flip chip mounted, multilayer ceramic decoupling capacitors have been developed by AVX Corp. for qualification and use by IBM Microelectronics. Under a new joint agreement between the two companies the LICA capacitor is available to the microelectronic industry. The recent innovations are performance modifications derived from the original design outlined by Humenik et al.[2] The first enhancement was an increase in overall capacitance from 32 nF to 100 nF, provided all four capacitors within the body are connected in parallel. The second innovation was twofold - the height of the barium titanate body without solder bumps was reduced to a nominal 0.65 mm (LICA low profile) with an associated increase in capacitance from 32 nF to about 56 nF. Extra capacitors plates were added to each of the 4 bundles to increase the number of plates from 8 to 12 per bundle and thus increasing capacitance. The distance between plates was also reduced, contributing to the overall increase in capacitance of each of the four sections for the 100 nF LICA and LICA low profile bodies. Below is a physical description of the finished body that highlights their differences where they exist.

Physical description*

Name	DCAP	LICA	LP-LICA
Capacitor	32 nF	100 nF	56 nF
C4 count	16	16	16
C4 pitch	0.4 mm	0.4 mm	0.4 mm
Width	1.6 mm	1.6 mm	1.6 mm
Length	1.85 mm	1.85 mm	1.85 mm
Height	0.875 mm	0.875 mm	0.650 mm
C4 diameter	0.125 mm	0.125 mm	0.125 mm
Dielectric **	T60T	T60T	T60T
Electrodes	Pt	Pt	Pt
Caps/body	4	4	4
nF/capacitor at RT and 1 KHz	8	25	14
# plates per body	32	48	48

Table 1.0. Physical Description of the Three Capacitors

Notes:

(*) - The description does not constitute a specification and represents a mixture of nominal, target and measured values as determined by IBM.

(**) - T60T is a formulation of barium titanate

2. Capacitor Fabrication

The process used to fabricate the three types of capacitors is similar and there are variations only in the overall dimensions, including body 'z' height as well as the number and size of internal electrodes. Fabrication starts with the use of a high-dielectric constant barium titanate-based ceramic insulator. This allows interelectrode layers to be sufficiently thick in order to enhance capacitor reliability by preventing dielectric breakdown. Other benefits of utilizing barium titanate-based ceramic is its resistance to chemical reduction[3], i.e. the capability of retaining a high dielectric constant at specific use temperatures and frequencies, as well as its manufacturing robustness in conventional capacitor fabrication. The internal electrodes used in conjunction with the barium titanate-based ceramic are platinum, which are formed as a result of subsequent metal paste screening and sintering with the compatible dielectric. The resultant electrodes and insulator are chemically stable as well as inert, and therefore can withstand reducing atmospheres required for the electrode wiring (termination) process. In addition, the resultant capacitors are resistant to corrosion and metal migration effects. The wiring, or termination process begins with the deposition of base metal Chromium (Cr). This is used for both electrode shorting through contact with the exposed tabs as well as the base adhesive interface of the substrate to the final interconnect metallurgy, the solder ball. Deposition of the initial chromium layer is achieved through use of the metal mask which defines the electrode interconnection in either a single, double or quad capacitor format, depending, on the application requirements.

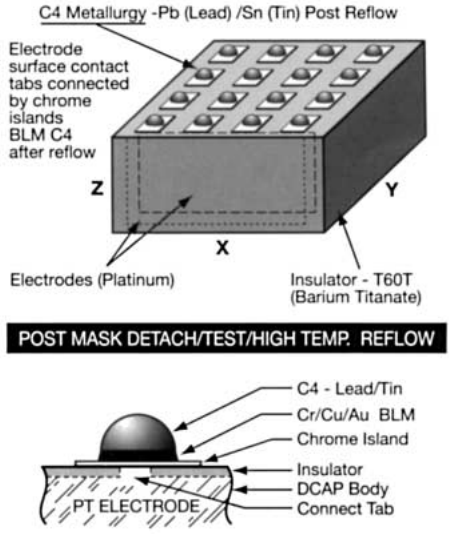

Figure 1. DCAP with Terminal Metals

The follow-on termination joining metallurgy is defined using similar masking techniques to construct the BLM (ball limiting metallurgy) base, which consists of the deposition of chrome-copper-gold (Cr-Cu-Au). This layer provides a wettable surface for the solder and also limits the solder movement, preventing flow onto the shorting Cr land(s). Final deposition of lead tin (Pb-Sn) metal alloy completes the termination/ interconnection joining structure. Post metal terminal deposition and subsequent fixturing/capacitor de-masking, melting of the solder alloy is achieved in a reducing atmosphere, forming the C4s, essentially similar to those used in semiconductor chip joining fabrication. Following solder reflow (melting), the capacitors are then electrically tested for capacitance and resistance of both internal electrode body and termination metal integrity. This is a very high yielding process, which is followed by a final visual inspection for any functional processing defects.

3. Module Process Assembly

The process for joining capacitors to MCM and single chip modules takes place in our bond, assembly and test facilities. The basic process flow is as follows:

- Load substrates in chip place tool to align and place flip chips (Universal).
- Flux is dispensed on the array of 16 C4's.
- The vision system performs a pattern recognition to the array of pads and C4's. It matches the patterns during the align sequence.
- The tool aligns and places the capacitors onto the fluxed sites.
- Flux holds the capacitors in position until the flip chip is placed and the hardware is reflowed in IR furnace purged with nitrogen or a nitrogen/ hydrogen mix.
- C4 solder joints are reflowed in an IR furnace in an atmosphere that reduces oxidation. Any slight misalignment is compensated for during reflow.

4. Reliabililty Evaluation

The three different capacitor body types were introduced into IBM module products and hence, qualified at three distinct time frames – the DCAP in 4Q'86, LICA in 1H'94 and LP LICA in 4Q'95. Reliability stress testing and electrical parameter characterization was done for each of the three designs.

4.1 DCAP (32nF) Capacitor

The thin film islands on the original DCAP design were a sandwich structure of Cr/CrCu 50-50 phased /Cu/Cr (layer 1 0.7 K°A/1.7 K°A/4.3 K°A/2 K°A). This structure was very susceptible to Cu Corrosion (C1) under Temperature Humidity Bias stressing. Consequently, the DCAP was confined to hermetic modules. In 2H'88, the thin film islands were changed to 1.2 K Ang. Cr (no Cu). The THB data reported below is from the qualification stress testing of the updated process. After the process change to all Cr thin film islands, DCAP usage restrictions were updated to include non-hermetic applications. For reliability stress tests, the DCAP capacitors were C4 joined to alumina ceramic substrates.

Summary of Reliability Stress Tests

1.0 Voltage Cycle at Room Temperature

- Stress: 0 - 15V bias cycling at rate of 72 cycles per day for 3500 cycles.
- Precondition: Thermal Shock, Impact Shock, Vibration (IBM Spec.).
- Sample: 48 capacitor chips (1/2 initial C4 join and 1/2 18 C4 reflows).
- Measurements: insulation resistance, capacitance, and plate resistance (redundant terminal to redundant terminal).
- Results: No failures.

2.0 TB (Temperature Bias) - 125C for 2.1 Khrs.

- Stress: 15V across plate terminals of 24 capacitor chips.
- Precondition: Thermal Shock, Impact Shock, Vibration (IBM Spec.).
- Measurements: insulation resistance, capacitance, and plate resistance (redundant terminal to redundant terminal).
- Results: No failures - no physical evidence of corrosion or metal migration or significant insulation resistance drift.

3.0 Temperature / Humidity (Cr Island Process Qualification)

- Stress: 85C/81%RH/6V DC Bias for 1000 hrs.
- Precondition: none.
- Sample: 24 biased DCAPS and 48 unbiased DCAP's joined to alumina ceramic substrates.
- Results: No electrical failures, no visual corrosion, no significant electrical parameter changes (capacitance, dissipation factor, and dielectric resistance).

4.0 Mil Std. Thermal Cycle (-55C/125C)

- Stress: 500 cycles at rate of 8 cycles per day.
- Precondition: none.
- Sample: 24 capacitor chips.
- Measurements: insulation resistance, capacitance, and plate resistance (redundant terminal to redundant terminal).
- Results: No fails or significant changes in measured parameters.

5.0 Thermal Cycle (0C/100C)

- Stress: 4800 cycles at 72 cycles per day.
- Precondition: Thermal Shock, Impact Shock, Vibration (IBM Spec.).
- Sample: 144 capacitor bodies stressed.
  For this test set, the island metallurgy pattern was modified, allowing two discrete capacitors within a body to be measured for capacitance, insulation

resistance, and plate resistance (redundant island to redundant island). Also two corner C4's per capacitor body had their resistance measured; thin film island resistance was also measured with the ring structure used for C4 measurements. Half of the parts were initial C4 joined while the other half were reflowed 18 times at solder melting temperature.

- Measurements: capacitance, insulation resistance, plate resistance and C4 resistance.
- Results: No failures.

6.0 Thermal Cycling (Cr Island Process Qualification)

- Stress: 0C/100C, 72 cycles per day (2000 cycles total).
- Precondition: none.
- Sample: 72 DCAPs joined to two alumina ceramic substrates. One substrate had one C4 join cycle and the other had 10 C4 join cycles prior to thermal cycling.
- Results: No failures or significant capacitor parameter changes or Cr resistance changes.

7.0 Tensile Chip Pull

- Sample: Substrates with joined capacitor chips had 1X, 10X, or 18X reflows prior to pull to failure (fail criteria was 1 pound).
- Sample size: 256 capacitor chips (3 nearly equal groups).
- Results: No failures to criteria.

8.0 Latent Defect Study

- Capacitors which had 2 defect types were stressed at 125C, 50 V bias, for 360 hrs.; leakage current was measured insitu. The two defect types were surface delaminations (AVX mfg. rejects) and surface cracks (perpendicular to plates on island face) which were artificially created by an indentation tool mounted on an Instron. Half of the capacitors in each defect group were soaked in boiling salt water prior to chip join, while the other half was not 'contaminated' with the boiling salt water.
- Sample: 2 groups of 12 capacitor chips joined to ceramic substrate which was capped. The matrix was:

'CONTAMINATED'	CRACKED	DELAMINATED
Yes	6 DCAPs	6 DCAPs
No	6 DCAPs	6 DCAPs

- Results: No significant change in insulation leakage at 50V (insitu measurements).

4.2 LICA (100 nF) Capacitor

The LICA C4 capacitor has the same external form as the DCAP, but has 4 additional capacitor plates per bundle (8 per bundle per DCAP vs 12 per bundle for LICA) and thinner dielectric between plates. Pt plate and dielectric thicknesses are the same as for the LICA low profile capacitor. The stress testing for LICA emphasized a shift in IBM reliability test strategy towards encompassing industry standard techniques as delineated in Mil. Std. 883D; LP - LICA included some JEDEC requirements but stress testing was not as rigorous as that for LICA because of its similarity to LICA. Qualification of LICA (100 nF) capacitor was performed in two phases. Phase One (T1) qualification consisted of a series of short reliability stresses, that would allow capacitors to be classified as potentially qualified (PQ level) upon successful completion. This phase requires a small sample size composed of capacitors already in-house. The second phase was composed of larger sample sizes and longer term stress tests, as well as a capacitor functionality evaluation, including the generation of the frequency dependence of capacitance, equivalent series resistance, equivalent series inductance and temperature dependence of capacitance. Physical analysis was also included.

Phase One reliability stress tests were performed in order as listed below. Sample size was 72 capacitors.

- Thermal Shock per Mil. Std. 883D/1011.9B, (15 cycles at -55C/125C, liquid to liquid).
- Moisture Resistance per Mil. Std. 883D/1004.7, 10 days.
- Thermal Cycle per Mil. Std. 883D/1010.7B, (500 cycles at -55C/125C, air to air).
- High Temperature Bias at 125C/50V for 168 hours.
- Results: No degradation in capacitance or dielectric resistance. Measurements were taken upon completion of each stress.

Summary of Phase Two Reliability Stress Testing

Three capacitor body lots (mfg. lots) were equally represented in the qualification.

1.0 Precondition sequence for all capacitor bodies C4 joined to alumina ceramic capped substrates.

- Purpose: to simulate worst case shipping conditions.
- T0 electrical measurements (capacitance, dissipation factor, and dielectric insulation resistance at 100V bias). Electrical measurements were per body (the 4 discrete capacitors on each body were connected in parallel with the substrate internal wiring).
- Liquid-Liquid Thermal Shock - Mil. Std. 883D/1011.9B, (15 cycles of -55C/+125C).
- Drill 2 holes in metal module cap to allow moisture ingress.
- Moisture Resistance Stress - Mil. Std. 883D/1004.7, (10 cycles, each lasting a day and ending with the 4 hrs -10 C step. A moisture stress like this was not done in the original DCAP (32 nF) qualification; instead impact shock and vibration testing was done - the author's view is that these stresses are benign.
- T1 measurements (same as T0 above).

2.0 THB (Temperature/Humidity/Bias) - 85C/81%RH/10 Volt Bias, 1000 hrs.

- Purpose: evaluate susceptibility of device to surface and internal electrode corrosion and metal

migration due to contamination effects incurred during manufacturing.

- Sample: 6 alumina ceramic capped substrates (12 capacitors joined to each substrate with each discrete in-chip capacitor having 10V bias applied between terminals).
- Precondition sequence (above).
- 1500 hours of stress with interim and post-stress room temperature measurements the same as at T0.
- No significant parameter degradation or failures.

3.0 TB (Temperature Bias - 125C/15V and 50V Bias/2 Khrs)

- Purpose: evaluate susceptibility to dielectric breakdown accentuated by the use of thinner dielectrics (compared to original 32 nF DCAP).
- Sample: 6 alumina ceramic substrates (12 capacitors joined to each substrate). Three substrates had their capacitors biased at 15V while the other 3 had capacitors biased at 50V.
- Precondition Sequence: 2000 hrs of stress testing with interim and post-stress room temperature measurements as at T0.
- Results: No significant parameter degradation or failures.

4.0 Thermal Cycling - Mil. Std. 883D/1010.7B (-55C/ +125C/No Bias/2000 cycles), Air-Air Sequence

- Purpose: evaluate susceptibility to crack propagation due to fissures/cracks advanced during preconditioning and due to platinum plate/barium titanate TCE mismatch and cohesion characteristics, and that of titanate/thin film island.
- Sample: 72 capacitors joined to six alumina ceramic capped substrates (12 capacitors joined to each substrate).
- Precondition Sequence (above).
- 2000 thermal cycles with interim and post-stress measurements as at T0. No significant parameter degradation or failures.

5.0 Thermal Shock - Mil. Std. 883D/1011.9C (-65C/+150C/No Bias/2000 cycles), Liquid-Liquid Sequence

- Purpose: evaluate the reliability of the Pt plate to thin film connection.
- Sample: 6 capacitor chips (2 from each body lot) attached to alumina ceramic plate for ease of handling and stressing. Electrical measurements were individual capacitor plate resistance (redundant islands to redundant island); 8 pairs per capacitor body. The resistance measurements were four point.
- T0 measurements.
- 2030 liquid-liquid thermal shock cycles with interim and post-stress measurements at room temperature.
- No significant change in island-island resistance.

4.3 LP-LICA (56 nF) Capacitor

1.0 TB (Temperature Bias - 125C at 15V and 50V Bias)

- Sample: 72 capacitors.
- Measurements: Capacitance, Dissipation Factor and Dielectric leakage.
- Precondition
  - Three passes through an IR furnace per JEDEC A113 Std.
  - Thermal shock per Mil. Std. 883D/1011.9B, 10 liquid to liquid cycles at -55/125C.
- Results: Increase in capacitance after three IR reflows by 1-2 nF per body. No significant change in parameters measured at end of stress.

4.4 Reliability Conclusions

Reliability stress testing for all three capacitor body types encompassed a wide variety of IBM and industry standard methods and revealed no significant failure or degradation mechanisms within the 'stress space' of these tests.

5. Electrical Characterization

5.1 LP-LICA Capacitor Electrical Characterization

1.0. Introduction

This paper describes the electrical characterization of the Low Profile LICA capacitor body individual discrete capacitors. The functional characteristics of the DCAP and LICA capacitors are similar except for values of discrete capacitor parameters and will not be discussed further in this paper. The evaluation of electrical characteristics is necessary in order to optimize module electrical performance during module design and to understand capacitor effects during module reliability burn-in and reliability testing. Three manufacturing lots of capacitor bodies were represented in the evaluation; 79 bodies or 316 discrete capacitors were tested in the various electrical tests. The thin film islands, which connect individual capacitor plates, were modified relative to the metal thin film stacks (thickness only, but not xy dimensions); the thin film metal islands were changed from Cr (1.2 K°*A*, normal for product) to Cr/CrCu/Cu/Au (1.6 K°*A* /1.4 K°*A* /4.3 K°*A* /10 K°*A*) to allow a thick low resistance 'cushion' for electrical probing; the thicker island is assumed to not significantly affect ESR (equivalent series resistance) measurements.

2.0 Sample Preparation

Discrete capacitor bodies were epoxied (side opposite thin film islands) to wooden dowel ends (3/32 inch dia. by 6 inches long) with a non-electrically conductive epoxy; wood was chosen for the dowel because of its thermal and electrical insulative properties. A thermocouple was epoxied to the side of each capacitor body; the thermocouples provided both temperature measurements and feedback control for an FTS (manufacturer) gas environmental unit. The FTS unit allows precise DUT (device under test) temperature

control. The unit impinges dry N_2 on the DUT (in this experiment, over the temperature range 0 °C to 100 °C). The dowels were held in a vertical position (capacitor body islands facing downward) to provide accessibility to a 2-terminal electrical probe attached to an impedance analyzer. Two different impedance analyzers were used and are listed in the equipment list. A camera/ TV system was used to enable probe positioning. All instruments were mounted on a steel air table to minimize mechanical effects (e.g., vibration and shock).

The equipment list is:

Instrument	Comment
HP 4291A Impedance Analyzer	1 MHz - 1.8 GHz
HP 4194A Impedance Analyzer	100 Hz to 40 MHz
Pico Probe (Model 40A-SG-400P)	DC to 40 GHz
HP Calibration Std.	Model 909D 50
Brinkman Manual XYZ Positioner	Model 06-00-71
Tesatast Dial Indicator	For monitoring probe overdrive
Keithley Micro-Ohmmeter	Model 500
FTS Gas Environmental unit	PAC TC-3-85-91

3.0. Electrical Measurements and Interpretation

The electrical parameters measured with the two impedance analyzers were based on the series circuit model for resistance, capacitance, and inductance. The measurements included ESR (equivalent series resistance), ESL (equivalent series inductance), ESC (equivalent series capacitance), self-resonance frequency (ω_{Res}), Z_{SR} (impedance at self-resonance) and dissipation factor (ω X *ESR* X *ESC*, where $\omega=2\pi v$ and v is frequency). Both ESR and ESC are functions of frequency and temperature, which is expected for a ferroelectric dielectric, as is dissipation factor since it is a function of ESR, ESC, and ω. ESR and ESC frequency and temperature dependencies are illustrated by examples for a given discrete capacitor unit. Statistical data is provided for all other parameters.

All of the measurements were 2-terminal (this was the electrical probe configuration), not 4- terminal. Each of the four discrete capacitors within a capacitor MLC (multi-layer ceramic) body have four terminals - two terminals for each plate set of a discrete capacitor (hence, redundant terminals). The statistics reported (mean μ and standard deviation σ) are for 2-terminal measurements; all data sets were fit to normal distributions. In order to convert this data to a 'real' module design configuration, where each discrete capacitor has its four terminals connected to two module or substrate power planes, one has to either model the 4-terminal and 2-terminal capacitor configurations in order to understand how to transform parameters from one type to the other or make assumptions on what the parameter transformations are. Modeling has not been done, but assumptions have been made for a set of transformations.

These are:

I. ESC is the same for both configurations.

II. ESR (4-terminal) = 1/2 ESR (2-terminal)

III. ESL (4-terminal) = 1/2 ESL (2-terminal)

IV. ω (Res/4-terminal) = $\sqrt{2}\ \omega$ (Res/2-terminal)

The second and third assumptions are based on the idea that each of the 2 sets of plates in a discrete capacitor has two redundant terminals which are used for charging and discharging. The characterization testing utilized only one of the two redundant terminals of each set. Hence, the resistances and current path lengths for the 4-terminal case are around 1/2 those for the 2-terminal case. For more precision, modeling is suggested. In calculating statistics for random variables, one can easily see that if one random variable is transformed into another by multiplying it by a constant, then the average and standard deviation of the new one is related to the average and standard deviation of the old one by the same constant, as shown below:

if $y_i = K \times x_i$

then $\bar{y} = K \times \bar{x}$

and $\sigma_y = K \times \sigma_x$

Assumption IV is derived from the assumption that if the 2-terminal inductance is halved, then the self-resonance frequency is shifted to greater values since at self-resonance the capacitive reactance equals the inductive reactance, or $1 \div \omega C = \omega \times L$, for C = capacitance and L = inductance.

3.1. Electrical Characterization Graphical Data

Following is set of graphs illustrating parameter distributions at 25°C and the dependencies of these parameters on other variables such as temperature, frequency, and voltage, where appropriate.

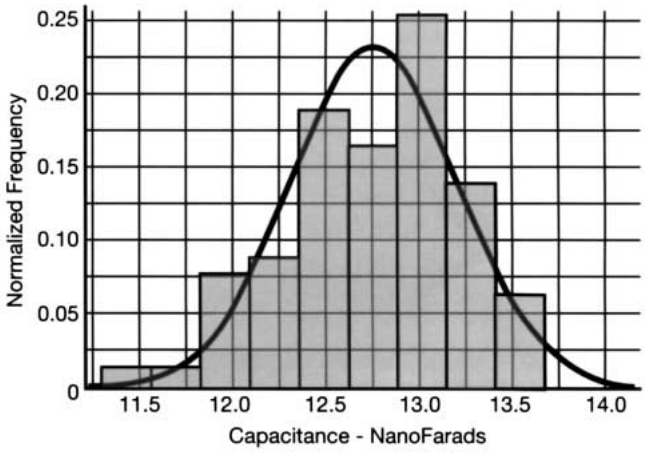

Figure 2. Histogram of Equivalent Series Capacitance at 25°C

This graph depicts the high frequency capacitance in the region below self-resonance where the frequency dependence is insignificant.

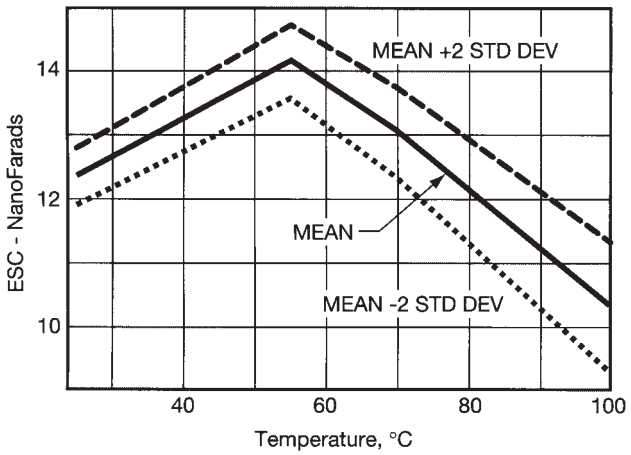

Figure 3. High Frequency Equivalent Series Capacitance vs. Temperature

This graph only connects the data points and is not a smooth function fit; hence inferences to intermediate temperatures may be somewhat conservative.

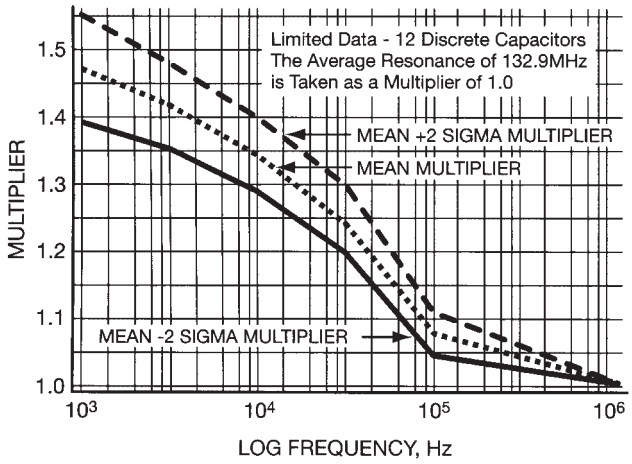

Figure 4. Series Capacitance vs. Frequency at 25ºC - Example

In the frequency region from about 50 MHz to self-resonance, the series capacitance is nearly independent of frequency. From DC to this region the series capacitance and resistance depends on frequency with the largest effects at the lower values. The above graph illustrates the multiplicative factor as a function of frequency (Multiplier = 1.0 for the base region noted).

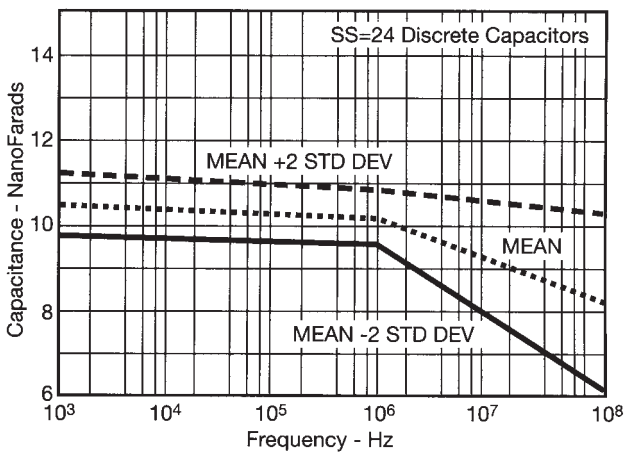

Figure 5. Series Capacitance vs. Frequency at 100ºC

Note that the frequency dependence is much less at 100ºC then at 25ºC, especially for the lower frequency range.

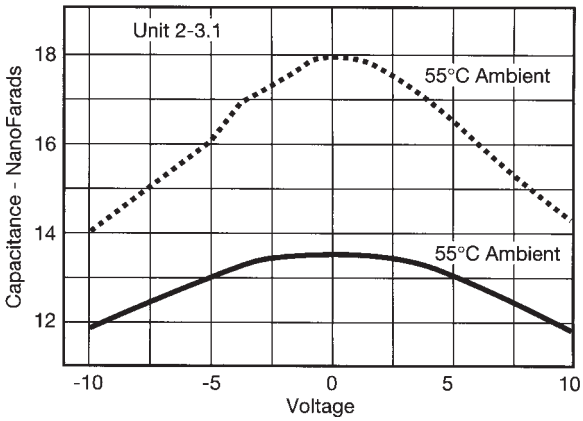

Figure 6. Equivalent Series Capacitance vs. Voltage - Example

Illustrated is ESC high frequency dependence on DC voltage for a single discrete capacitor. All previous charts for ESC are for zero volts DC voltage during the measurements; the AC test signal voltage was 1.0 VRMS for all measurements.

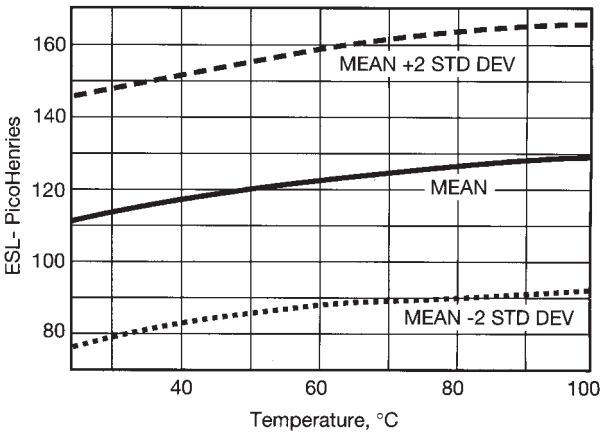

Figure 7. Equivalent Series Inductance vs. Temperature

No evidence has been generated that indicates inductance is a function of frequency. Voltage dependence, if any, was not addressed.

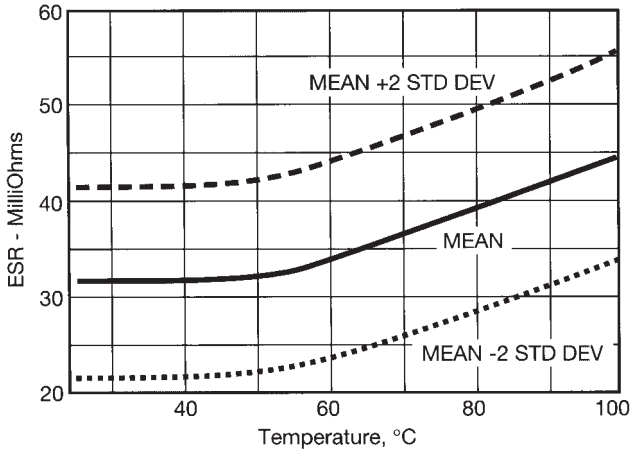

Figure 8. Equivalent Series Resistance vs. Temperature

ESR at self-resonance is presented here; at this point ESR has values comparable to the DC resistance of the capacitor plates. Because each plate set for each discrete capacitor in a capacitor body has two terminals, the plate resistance can be measured explicitly.

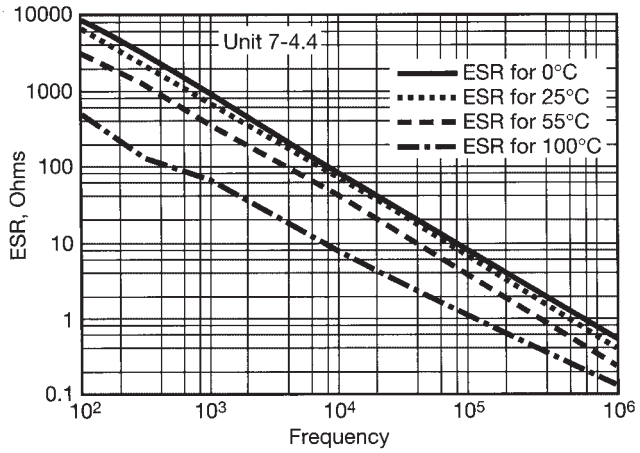

Figure 9. Equivalent Series Resistance vs. Frequency and Temperature

Series resistance is a function of frequency. This graph illustrates an example of such behavior for one unit.

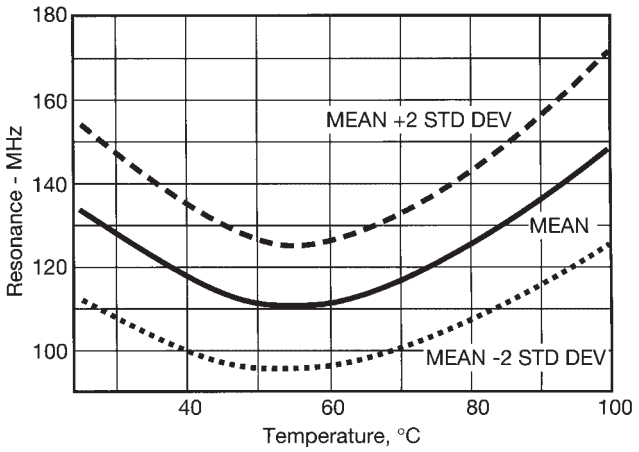

Figure 10. Self-Resonance Frequency vs. Temperature

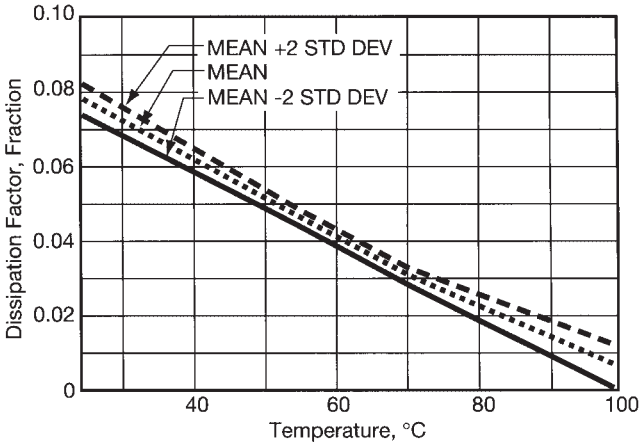

Figure 11. Dissipation Factor vs. Temperature - 1 KHz

The parameter, dissipation factor, was measured with the impedance analyzers at 1 KHz and 1 MHz; these measurements are consistent with the formula

$$DF = 2\pi \times \omega \times R \times C$$

where R and C are the series resistance and capacitance at ω.

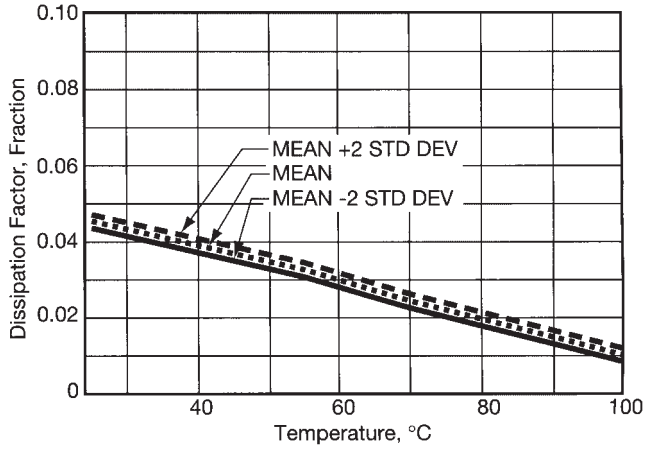

Figure 12. Dissipation Factor vs. Temperature - 1 MHz

3.1.1 Summary - Electrical

Capacitor electrical parameter (based on series RLC model configuration) distributions and dependencies on temperature, frequency, and DC bias were presented for the Low Profile LICA Capacitor. The DCAP (32 nF) and LICA (100 nF) C4 bumped capacitors have the same functional dependencies but different initial room temperature values. Because these capacitor types have ferroelectric dielectric materials, the capacitance peaks at the critical or Curie temperature (about 55°C) for any given frequency. Capacitance values are frequency dependent which decrease as frequency increases. The electrical parameters were measured with a 2-terminal probe, and the values were not converted to 4-terminal equivalents. However, a set of assumptions was proposed which will allow such a conversion. If more accurate transformation is desired, it is proposed that analytical modeling be done to provide it. Measurements were generally recorded for discrete temperatures, voltages, and frequencies. Values at intermediate points can be estimated by extrapolation.

5.2 DCAP Capacitor Electrical Characterization

1.0 Capacitance vs. Temperature

- Sample size: 12 DCAP's joined to alumina ceramic substrate.
- Results: Description of envelope for capacitance (nF).

TEMP.	-70°C	22°C	60°C	140°C
C (high)	4.3	9.3	11.6	4.3
C (low)	3.5	7.7	9.4	3.5

Table 2. High and Low Values of Capacitance (C) vs.Temperature

2.0 Capacitance Measurements at Liquid Nitrogen Temperatures

Twelve DCAP capacitor chips were joined to alumina ceramic substrates and measurements (capacitance and dissipation factor) were made at room and liquid nitrogen temperatures. The parts underwent two liquid nitrogen cycles and exhibited no parameter degradation.

	CAPACITANCE (nF)		DISSIPATION FACTOR (%)	
	Average	Std. Dev.	Average	Std. Dev.
Room Temp.	8.056	0.174	4.35	0.17
LN. Temp.	0.873	0.029	5.61	0.05

Table 3. Capacitance and Dissipation Factor at Room and Liquid Nitrogen (LN) Temperatures

Note that the capacitance at liquid nitrogen temperature is about 11 % of the room temperature value. Measurements were at 10 KHz and 1 VRMS with an HP 4275A LCR meter.

6. Physical Analysis

Physical analysis of representative DCAP, LICA and Low Profile LICA capacitors was performed. Of particular interest was the physical arrangement of the Pt plates in the matrix of $BaTiO_3$, the presence or absence of gapping between the $BaTiO_3$ and Pt and mechanical integrity of the assembly. Representative samples of each type of assembly were analyzed. Further, for the Low Profile LICA capacitor, representative samples from 3 separate lots were provided for the analysis.

Characterization of the physical arrangement of the Pt plates with the $BaTiO_3$ was accomplished by a series of horizontal cross sections (top, middle, bottom) through the body of the assemblies. Each section was then examined in an SEM and measurements were taken.

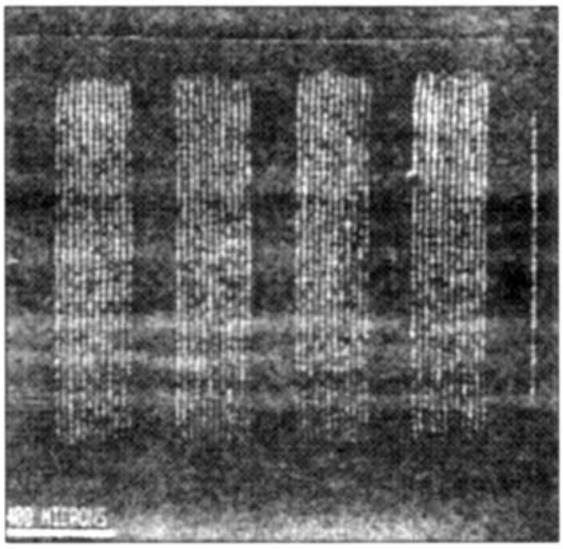

Figure 13. Micrograph of Internal Arrangement of Pt Plates within a Typical Low Profile LICA

Figure 13 is a micrograph of a representative section taken through the middle of a Low Profile LICA. For the LICA capacitors the plates are bundled into 4 groups of 12 plates each. For the DCAP's the plates are bundled into 4 groups of 8 plates each. The length of the plates ranged between 1.30-1.33 mm. The width of the groups of plates was between 210-220 µm at the ends and 230-240 µm near the middle. The outer plates in a group tended to be slightly more curved at the ends compared to the plates nearer the center of the group (Figure 14).

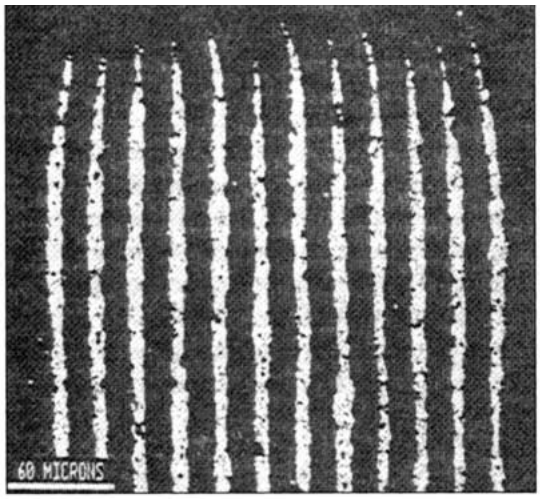

Figure 14. Micrograph Showing Typical Curvature of Pt Plate Ends

Figure 15 is typical of the amount of contact and gapping found in both the LICA capacitors and the DCAP. The arrangement of the plates and the spacing at each level of sectioning was consistent indicating that the plates were resonably parallel top to bottom. In general the thickness of the Pt plates were between 4-9 µm with a minimum of 0 µm on a local basis to maximum of 18 µm in the case of a small area on one Pt plate. The typical thickness of the $BaTiO_3$, between the plates on the LICA capacitors ranged between 14-18 µm. The minimum dielectric measured was 10 µm and the maximum thickness measured was 35 µm.

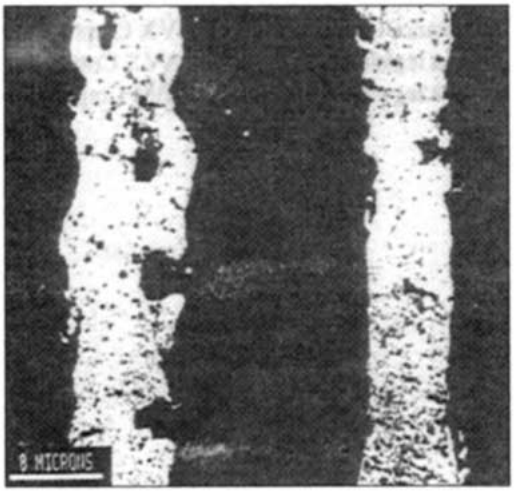

Figure 15. Cross Section Showing Usual Extend of Pt to $BaTiO_3$ Contact

For the 8 plate groups found in the DCAP's the typical Pt plate thickness was 7-10 µm while the dielectric thickness was found to be between 24-28 µm. In general it was found that there was reasonable contact of the dielectric with the Pt plates. In some cases sharp curved gaps were found extending from the ends of some Pt plates into the $BaTiO_3$ (Figure 16). Although this raised concerns that these sharp gaps might act as crack nucleation sites, no evidence was found of such occurrences.

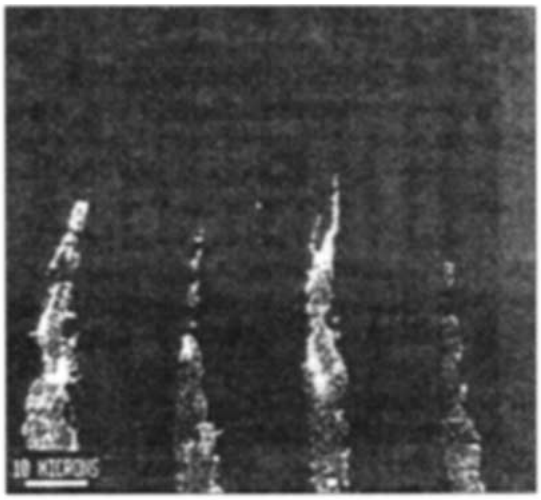

Figure 16. Micrograph of Sharp Curved End Gaps Found at the End of Some Pt Plates

The mechanical integrity was assessed by fracturing the assemblies and assessing their failure modes. A measure of goodness was determined to be indicated by fractures that did not appear to be dominated by a Pt plate to $BaTiO_3$ dielectric interface fail. The assemblies were fractured by gluing studs onto the sides parallel to the plates of the assemblies and applying an increasing axial tensile load until the assembly failed. Due to the difficulties of aligning the studs with the axis of the assemblies no attempt was made to quantify the load or stress at which failure occurred. All 4 of the LICA capacitors had acceptable modes of failure.

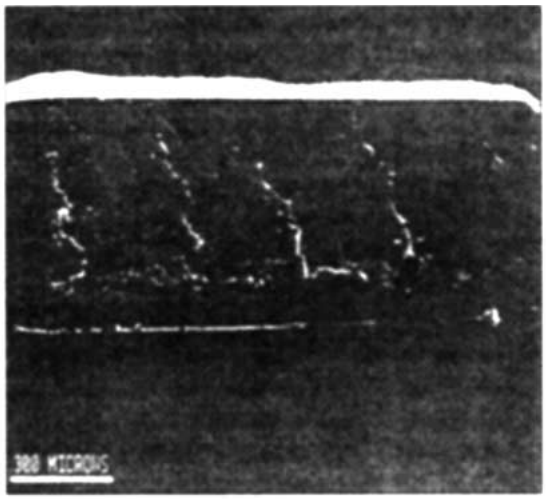

Figure 17. Micrograph of Acceptable Failure Mode with Fracture Mode Running Over Several Pt Plates

Figure 17 shows a typical failure surface. As can be seen in the micrograph, the fracture runs through numerous layers of the Pt plates and $BaTiO_3$ dielectric and does not concentrate along any one particular interface. Figure 18 shows a less desirable fracture that occurred in the DCAP. In this particular instance the fracture was predominantly along the Pt to dieleetric interface of two adjacent plates.

Figure 18. Micrograph of the Less Desirable Failure Mode with Fracture Running Over only Two Plates

X-ray diffraction was used to identify the phase(s) present. Samples were mounted on a Rigaku model PSPC-MDG x-ray microbeam diffractometer. A 100 µm diameter beam was centered on the capacitor. A diffraction pattern was collected using copper radiation (Beta-filter) from a rotating anode generator operating at 50 kV and 200 mA. The total scan time was one hour. Comparison of the patterns obtained showed all to be equivalent with predominant phase being $BaTiO_3$. There was evidence in the patterns for one or more minor phases: the identity of the minor phases could not be established.

7. Summary

Reliability stress testing indicated highly reliable capacitor for most computer product applications where the capacitor is joined to ceramic substrates (hermetic and non-hermetic electronic modules). The LICA capacitor family (DCAP, LICA and LP-LICA) capacitors have the same basic material set, construction and manufacturing process with some minor differences. The most essential difference between family members is capacitance value. The LP-LICA characterization data is presented to illustrate essential parameters (ESC, ESL, ESR, dissipation factor and self-resonance frequency) and their dependencies on major variables (temperature, frequency and voltage). The electrical data of the high K dielectric capacitors can be used to optimize electronic module design and to understand the role of the capacitors in manufacturing process steps, such as module test and functional burn-in.

IBM has successfully introduced MCM, MCM-D and SCM products built with DCAP's with a nominal rated capacitance of 32 nF and 100 nF. Currently our flagship RISC 6000 based work stations, high end CMOS main frames and AS400 midrange systems boast excellent low noise performance. Both TCM[4] and Glass Ceramic electronic packages[5] found in the Enterprise System/9000 and 3081 (bipolar chip technology), respectively, provide a history of zero defect performance relating to the AVX/IBM capacitor spanning over 10 years.

Reference

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2. J.W. Humenik et al. "Low inductance decoupling capacitors for the thermal conduction modules of the IBM Enterprise System/9000 processors", IBM J. Res. Dev. Vol. 36, No. 5, September 1992
3. J.M. Oberschmidt and J.N. Humenik, "A Low Inductance Capacitor Technology" Proceedings of the 40th Electronic Components and Technology Conference, IEEE, 1990, pp. 284-288.
4. Albert J. Blodgett, Jr., Scientific American, W.H. Freeman and Company, NY, Vol. 249, No. 1, pp. 86-96.
5. IBM J. Res. Dev., Vol. 36, No. 5, Sept. 1992, pp. 817-955, cover photo of substrate populated with DCAP's

   LICA Procurement specification by J. Galvagni, AVX Corporation.

   Low Inductance Capacitor Arrays, AVX Corporation.

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