TECHNICAL PAPER

Some Observations on Recent MLCCs Quality as Experienced in Europe

Including Discussion of Two Types of Dpa Analysis

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Abstract

A study of the European MLC quality by two types of DPA analysis shows that the newer formulations of 2F4 (Z5U) are as reliable as C0G (NP0) and 2C1 (X7R) formulations. These newer 2F4 formulations have small grain structure and low porosity which perform excellent on life test at 2xRV and load humidity 85ºC/85% RH at RV.

SOME OBSERVATIONS ON RECENT MLCS (MULTILAYER CERAMIC CAPACITORS) QUALITY AS EXPERIENCED IN EUROPE, INCLUDING DISCUSSION OF TWO TYPES OF DPA ANALYSIS

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Introduction

Samples were obtained of several types of MLCs from recent production of various suppliers into the European market. An effort was made to obtain surface mountable chips terminated with Nickel Barrier leach resistant material.

These units were sectioned and examined by standard DPA (Destructive Physical Analysis) as mainly recommended by EIA document RS469. Chips were further analyzed by a fracturing/scanning electron microscope technique developed in the Coleraine laboratories.

Leach testing was carried out to a severe criteria (260°C in 60/40 solder for a maximum time of two minutes, 100% coverage). Chips were also subjected to 85°C/85% RH (Relative Humidity) life test as well as standard temperature/voltage life tests.

It is the intent of this paper to show how current MLCs, in the case of the better makers, are extremely tough reliable units well adapted to the requirements of SMD (Surface Mount Devices). It will also show how they are being manufactured in much higher values than formally possible and the doubts often expressed about the quality of Class II ceramics are no longer viable.

Destructive Physical Analysis (DPA)

EIA RS469

This excellent document goes a long way to prepare the analyst for the pitfalls in trying to correctly carry out the difficult task of grinding and polishing sections of ceramic capacitors in order to identify possible defects in structure and manufacture. It rightly points out the ease with which defects can be induced by the techniques used. With the best will in the world it cannot be said that RS469 is amenable to day in day out DPA on a large scale (at Coleraine examine about 2000 sections a day), due to the constraints put on the analyst in terms of preparation of the sample and the care taken in grinding/polishing.

With some alterations to speed up the process it can however accurately identify some defects.

Table I. *List of defects which quick DPA polishing/grinding can/cannot identify.*

	YES	NO
Bad orientation of margins/electrodes	*	
Thickness of dielectric	*	
Thickness of electrode		*
Details of termination**	*	
Porosity		*
Grain size		*
Cracks	?	?
Corner rounding	*	
Delaminations	Invariably accentuated	
Voids	Similar to delams	

**Termination details can be seen by "filling" the resin with some hard material (e.g., zirconia) this avoids "section/resin relief" by making the support as hard as the section (Fig. 3).

SEM/Fracture

If the chips are mechanically fractured and examined with a scanning electron microscope a wealth of information not available by polishing and grinding can be obtained. The large depth of focus of the EM together with the ability to acid etch the sample so showing grain size easily, result in a good quality almost undisturbed image (except for cracks) to be viewed and interpreted.

Table II. *List of defects that SEM/fracture can/cannot identify.*

	YES	NO
Bad orientation of margins/electrodes	*	
Thickness of dielectric	*	
Thickness of electrode	*	
Details of termination	?	?
Porosity	*	
Grain size	*	
Cracks	?	?
Corner rounding	*	
Delaminations	*	
Voids	*	

Comparison of SEM & RS469

To illustrate these features the following photographs are shown. In many cases one chip has been fractured in half–one half being set in resin and ground/polished, the other half mounted and gold sputtered. The first half was photographed from a Nikon Optiphot image; the second was photographed from the CRT of a Jeol 200 SEM.

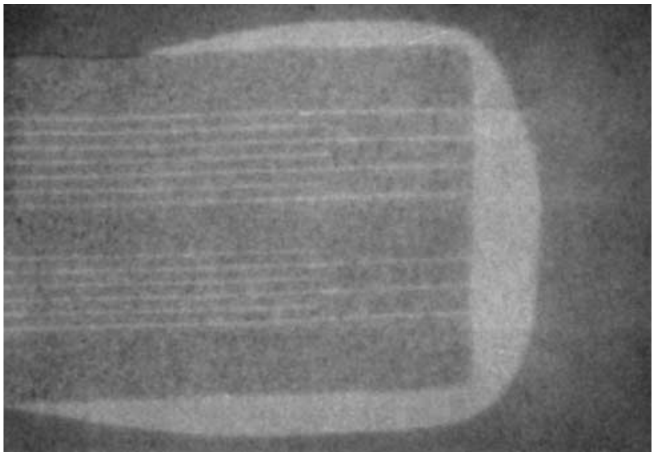

Figure 1. Normally polished section.

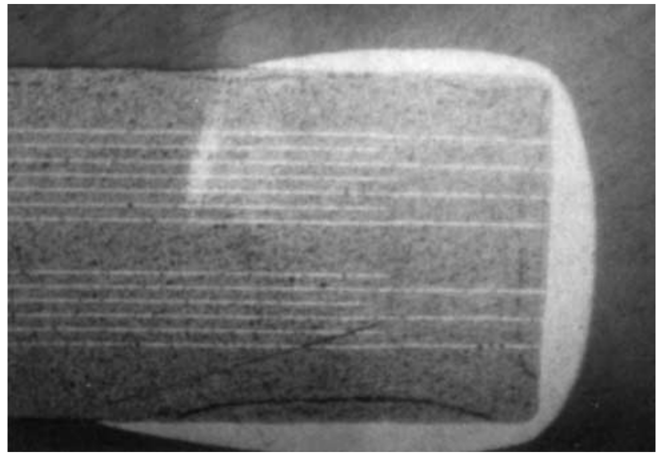

Figure 2. Crack induced (same chip) by poor polishing.

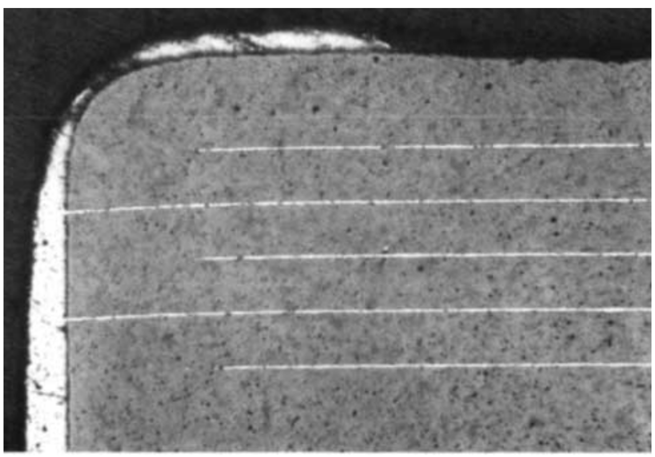

Figure 3. Polished section, out of focus edge induced by non filled resin.

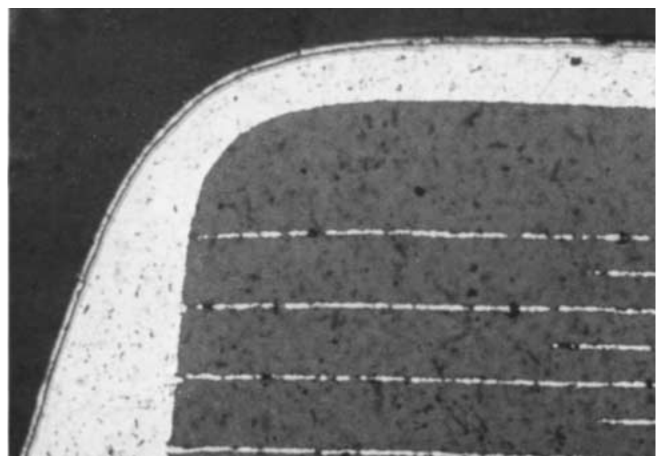

Figure 4. Polished section, sharp edge focus due to Zirconia filled resin (Barrier layer shown).

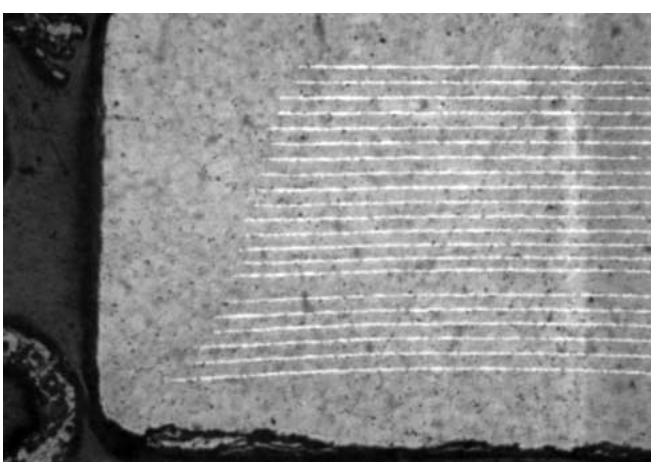

Figure 5. Polished section correctly showing poor side margin (slipped stack).

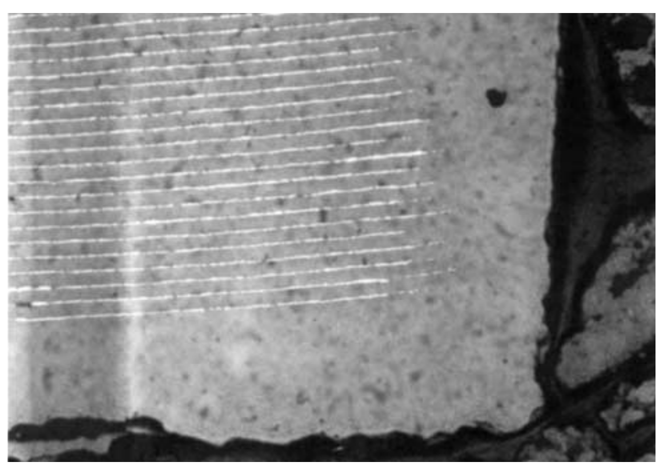

Figure 6. Polished section correctly showing poor side margins (angle cut).

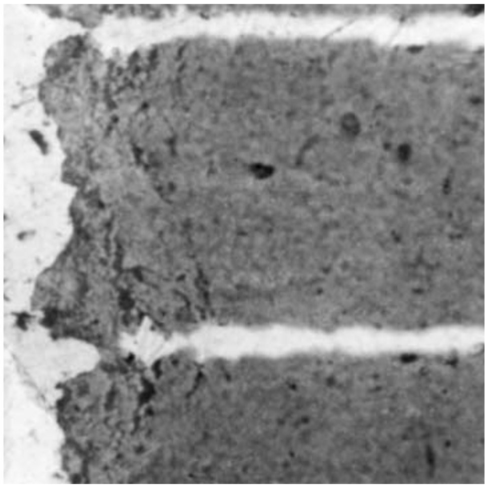

Figure 7. Polished section showing poor detail of micro cracks at termination.

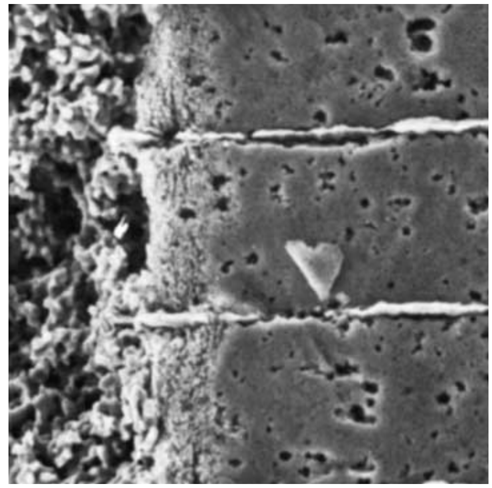

Figure 8. Fractured/SEM section showing better detail of micro cracks.

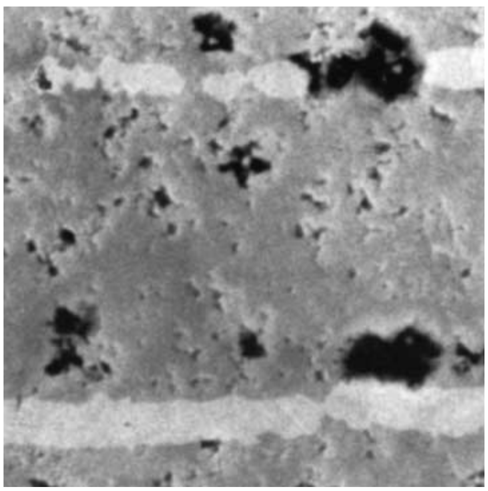

Figure 9. Polished section apparently showing bad porosity and poor grain ‘structure.

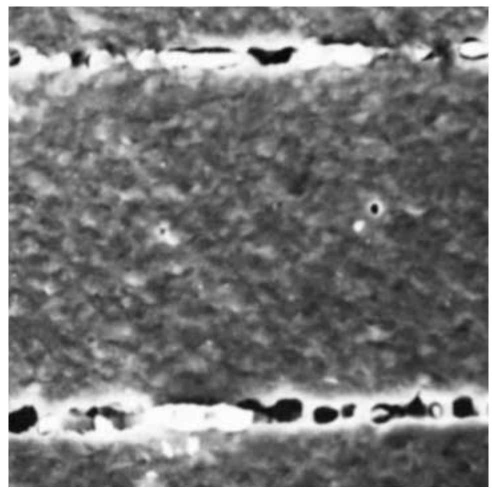

Figure 10. Fractured/SEM section of same chip showing correct picture of porosity free structure.

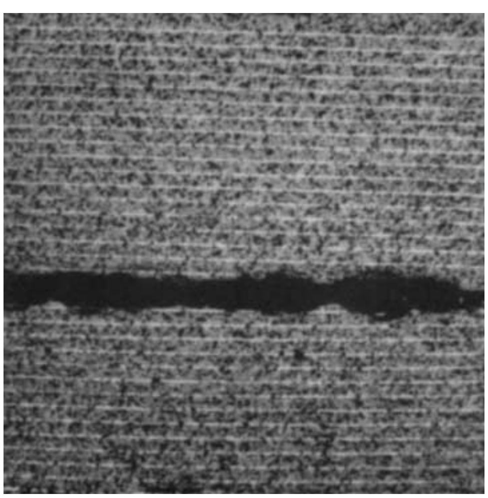

Figure 11. Polished section showing bad delamination voids.

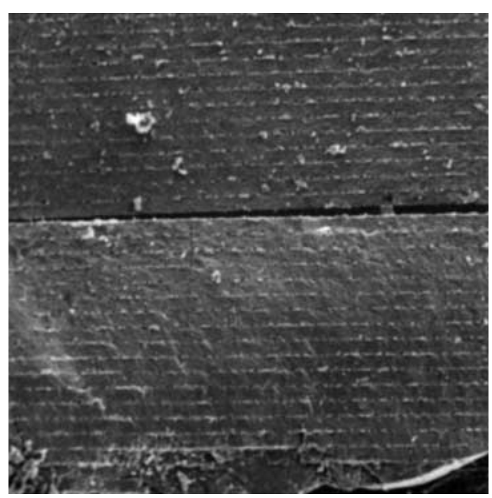

Figure 12. Fractured/SEM showing true appearance of a delamination.

DPA Results on Various Dielectric Types

General

Quality performance of the several types of MLCs Class I C0G (NP0), 2C1 (X7R) and Class II 2F4 (Z5U, Y5V) has generally been considered to be in direct order of temperature stability and inverse order volume effectiveness.

For example, a NP0 MLC with essentially no temperature variation of capacity and a “K” value of 70 has been considered a higher quality part with regard to life test and internal structure than a 2F4 type with a wide temperature/capacity variation and a “K” value of 10,000. This is derived from the knowledge that NP0 ceramics have a fine grain high dielectric strength, low porosity structure which is very safe as regard to penetration of moisture, voltage breakdown and defect structure which could allow conduction between opposite electrode layers and thus failure of the capacitor at some time in its life. This has been taken to heart by some users who will not use 2F4 (Z5U) material at all, even for decoupling, an X7R capacitor being specified. This user will then not be designing effectively as he is using a capacitor which is larger and dearer than the correct capacitor for the circuit. At one time this was not an unreasonable thing to do due to the poor performance of some manufacturers’ Z5U parts. Over the past few years things have changed. Some of the manufacturers by careful research work have developed fine grain, low porosity, high dielectric strength, high “K” value ceramics fully as reliable as the older low K ceramics. Further, in order to achieve consistent homogeneity and thus consistent processing conditions, the following have been addressed:

(a) Pre-reaction of individual components before grinding

(b) High purity sources of individual components

(c) Adjustment of stoichiometry to achieve better process windows.

(d) Careful work on each batch of Barium Titanate to equalize variations of this basic raw material.

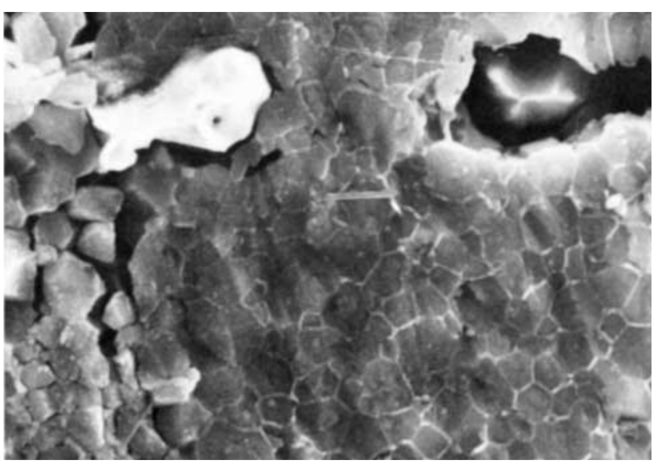

Figure 13. “New” technology fine grain 2F4 (Z5U) 1700x mag., acid etched.

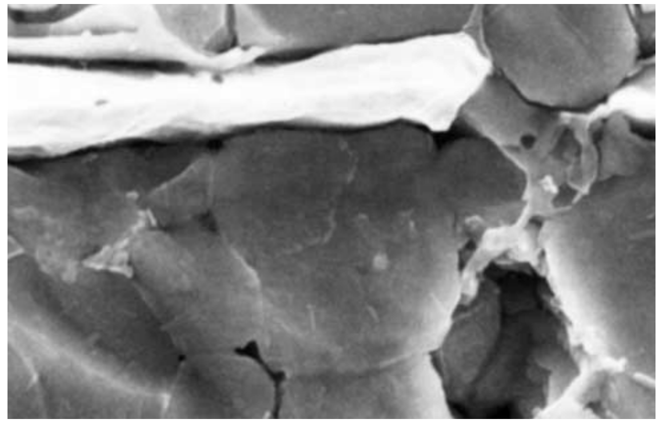

Figure 14. “Old” technology coarse grain 2F4 (Z5U) 1700x mag., acid etched.

In AVX this has enabled us to achieve life test data on 2F4 material of an aging rate of 1% per decade, “K” value of approximately 10,000 and an average voltage breakdown on a 0805 0.1 microfarad part of 800 V.

Similar work has been done on 2C1 (X7R). The following micrographs from SEM images show how various manufacturers at present supply into Europe with C0G (NP0), 2C1 (X7R) and 2F4 (Z5U) material. Some of the micrographs are acid etched to show grain structure and the extent of the glass frit/termination electrode interfaces, this must be borne in mind when looking at the micrographs. The main differences which show up on these micrographs is that of porosity and grain size. The connection is made here that it is better to have a small grain size and a low porosity than vice versa. If any porosity is present, it should not be connected pores. The mechanism of failure under high humidity conditions or on extended life test is thought to be conduction of some kind with the assistance of moisture along spaces at the grain boundaries of large grains and/or through connected pores.

To test this 85°C/85% RH high impedance and standard life test were carried out on parts which were considered good and poor from the DPE SEM analyses. Six manufacturers’ parts were examined.

Selections have been made by the author to show what he believes to be “old” technology and “new” technology. Manufacturers have been identified by A, B, C, D, E, and F.

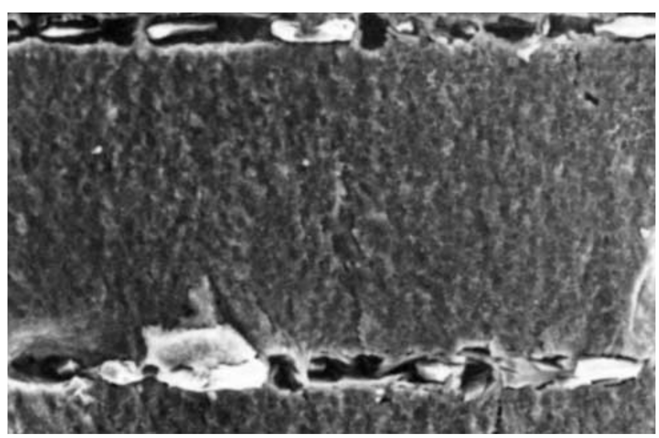

Figure 15. Manufacturer A 2F4 (Z5U) fracture/ SEM 700x mag. Excellent dense structure.

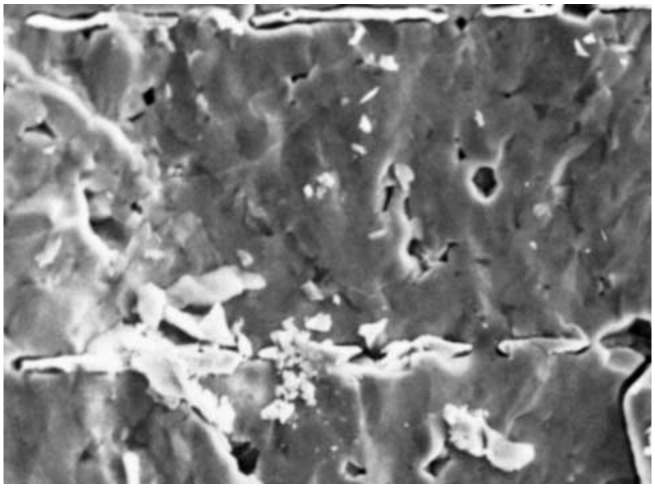

Figure 16. Manufacturer B 2F4 (Z5U) fracture/ SEM 700x mag. Some porosity and large grain showing.

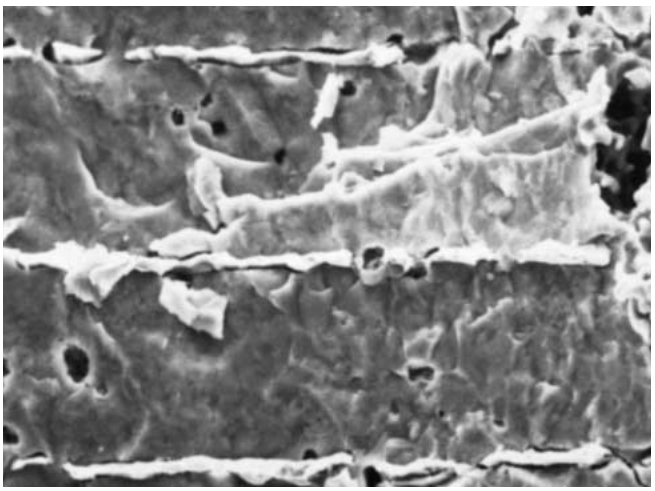

Figure 17. Manufacturer E 2F4 (Z5U) fracture/ SEM 700x mag. Some porosity and large grain showing.

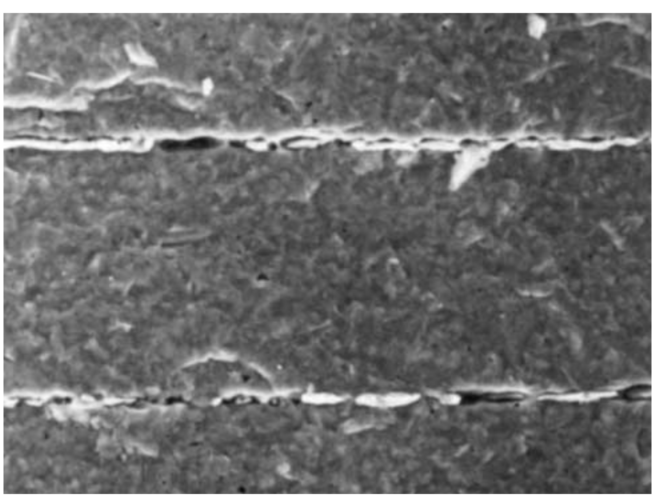

Figure 18. Manufacturer B C0G (NP0) 700x mag. Good structure.

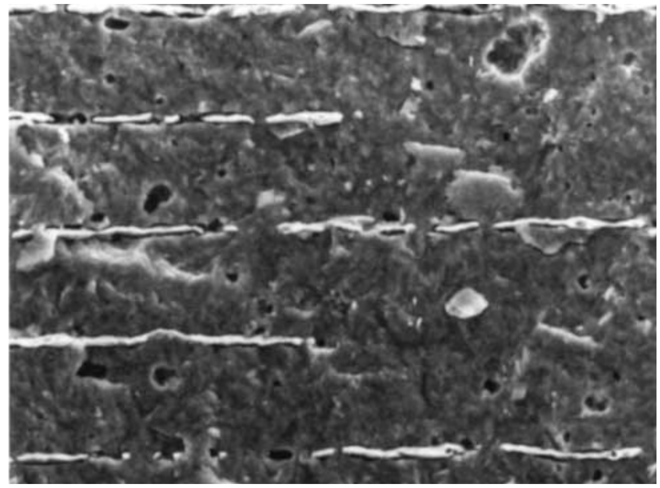

Figure 19. Manufacturer E C0G (NP0) 700x mag. Good structure.

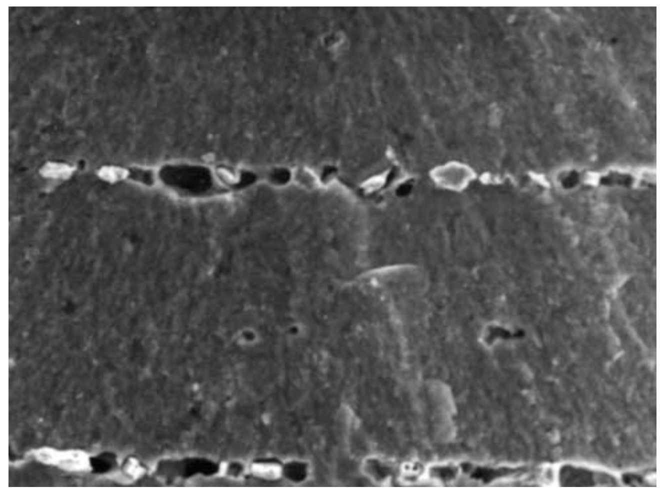

Figure 20. Manufacturer A 2C1 (XR7) 700x mag. Good structure.

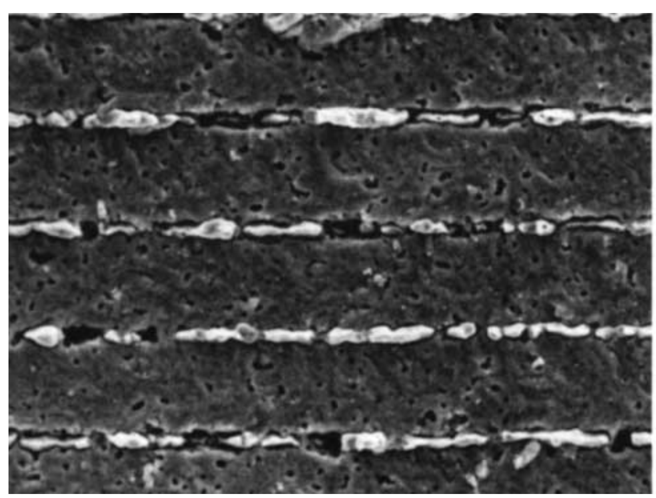

Figure 21. Manufacturer C 2C1 (X7R) 700x mag. High porosity, thin dielectric.

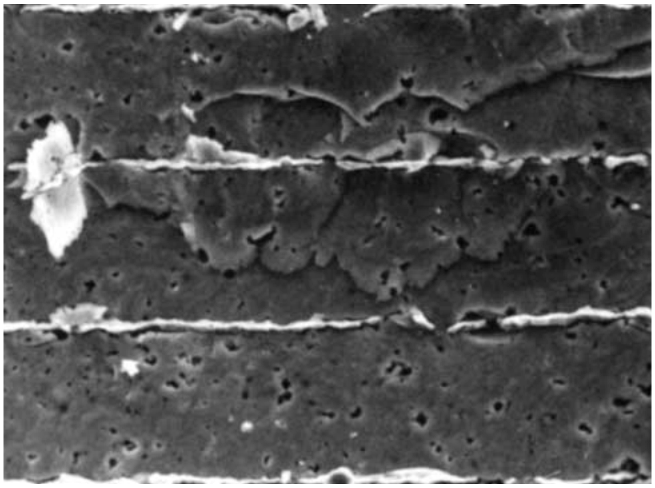

Figure 22. Manufacturer E 2C1 (X7R) 700x mag.
Some porosity.

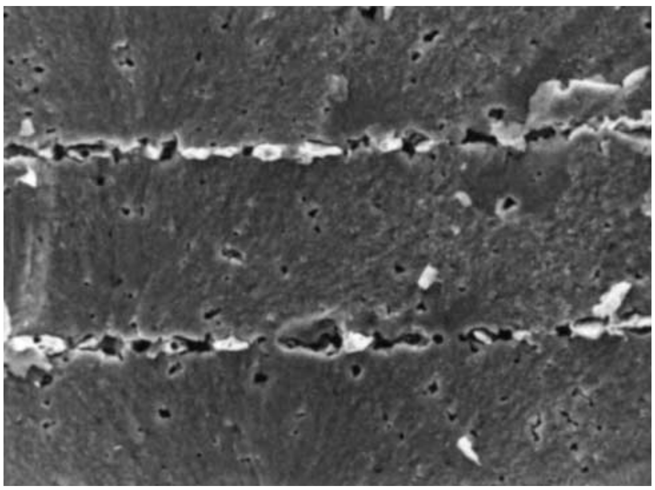

Figure 23. Manufacturer F 2C1 (X7R) 700x mag.
Some porosity.

Life Tests

Two sets of life tests were carried out.

(1) 85% RH/85°C with 50V DC applied across parts and 6.8 K ohms resistor. Great care was taken that there was no 100% moisture present at any time. Jig was carefully designed so that there were no failures due to tracking on the jig. This combination was chosen because after consultation with AVX customers this was the most representative condition of failures of some manufacturers' parts in the past (surface mount chips).

(2) Oven life test at 125°C (C0G, 2C1) at 85°C (2F4) twice rated voltage (10OV). This represented standard life test conditions as practiced by AVX.

A brief summary of results is given in Table III of manufacturers A, B, and C. It should be noted that it was impossible to do large numbers of parts and hours which really are needed for accurate results; a trend, however, is shown.

Failures out of 80 parts put on test for 1000 hours are shown:

Table III.

		FAILURES 85/85	FAILURE STD LIFE
MAN A	C0G	NIL	NIL
	2C1	NIL	NIL
	2F4	NIL	NIL
MAN B	C0G	NIL	NIL
	2C1	2 (IR)	NIL
	2F4	1	NIL
MAN C	C0G (DF, IR)	13	5 (Cat)
	2C1 (Catastrophic)	2	1 (Cat)

In general these results do show some comparison with ceramic structure, manufacturers A and B being a good deal better than C. They also show the higher severity of the 85/85 test even with lower temperatures and lower voltages applied. Moisture having a considerable acceleration factor.

Leach Tests

Nickel barrier terminations were available from manufacturers A, B, D, and F. Leaching tests were done with stationary chips in 60/40 solder at 260°C for two minutes. All but one manufacturer passed the test. The one manufacturer who did not pass at two minutes passed after one minute immersion.

The two manufacturers' samples which did not have a barrier termination were doubtful at only 20 seconds.

Summary

MLC surface mount chips as supplied to European users from manufacturers with up-to-date ceramic processing techniques are extremely reliable devices.

The successful manufacture of these parts with good yields and life tests indicates the progress that has been made in the manufacture of MLCs. Standard routine parts are now extremely reliable devices with very low incidences of failure in the field. They are also tough, robust devices well adapted to the sometimes searching procedures of surface mount. Indeed, because of the reduction in steps in producing the finished product in surface mount (no lead soldering, encapsulation or extra testing is required), the final product as regards capacitors should be even more reliable.

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