TECHNICAL PAPER

Surface Mount Soldering Techniques and Thermal Shock in Multilayer Ceramic Capacitors

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Abstract

All components used in surface mount assemblies have temperature processing limitations that must be adhered to for maximum reliability. This paper discusses multilayer ceramic capacitors in detail and soldering process considerations that are valid for all SMT components.

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SURFACE MOUNT SOLDERING TECHNIQUES AND THERMAL SHOCK IN MULTILAYER CERAMIC CAPACITORS

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Surface mount manufacturing promises tremendous advantages in product density, automated assembly and improved electrical performance but the components are directly exposed to soldering temperatures where the thru hole counterparts are not. This direct exposure causes reliability problems when the rate of rise in temperature is too rapid due to the inability of mechanical stress to be spread throughout the component. This is compounded by differences in coefficients in thermal expansion (CTE) and thermal conductivities (δ_T) of materials used in the construction of electronic parts. Multilayer ceramic capacitors (MLC) which are one of the most commonly used SMD, are among those components sensitive to thermal shock and will be discussed in detail. Figure 1 shows a cross section of an MLC with typical CTE and δ_T listed for the termination, ceramic body and electrodes.

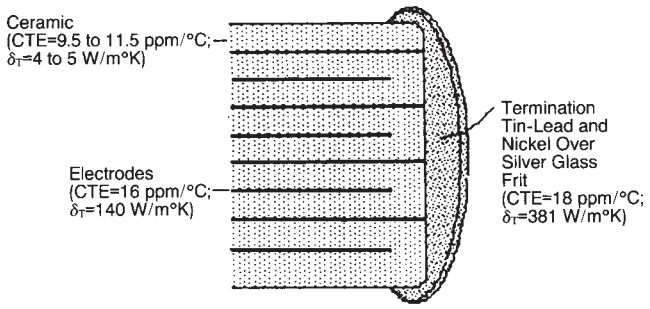

Figure 1. MLC Structure with CTE and δ_T Listed

The termination and electrodes heat up more quickly than the ceramic body, exerting forces on the ceramic which cause cracking if the temperature rate of rise is too rapid. This is due to a large difference in CTEs and δ_T between the ceramic and termination. As the termination heats up, it is an expanding rectangular annulus pulling on the ceramic while the expanding electrodes act as wedges forcing the ceramic apart at the electrode/termination interface as shown in Figures 2 and 3.

Different soldering techniques impact temperature rates of rise by the heat transfer mechanisms that are used. Wave soldering uses liquid metal which has the highest heat transfer rate and is the hardest soldering method to use without shocking any SM component.

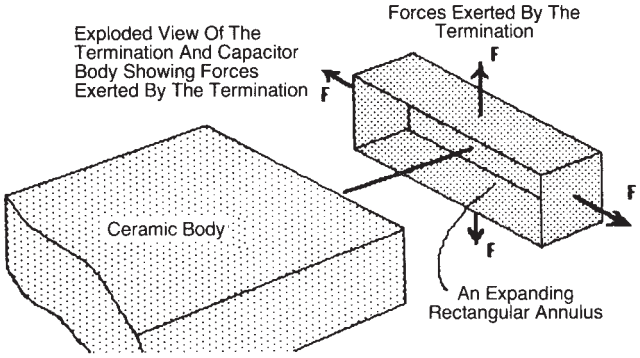

Figure 2. Forces Exerted by the Termination on the Ceramic Body

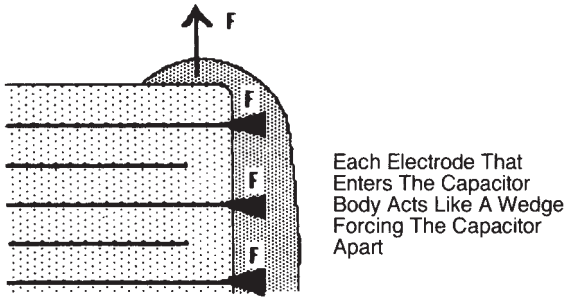

Figure 3. Temperature Forces that Stress an MLC's Structure

Vapor phase reflow (VPR) soldering uses latent heat of vaporization of the condensing vapor as the heat transfer method. Thermal shock of components is not obvious when VPR soldering is used but it can still be present. Hot belt reflow and infrared (IR) reflow have lower heat transfer rates because conduction, convection and radiation are the heat transfer methods used.

Wave soldering has the highest heat transfer rates and puts the greatest thermal shock stress on components. When extreme thermal shock is present, it is very obvious with visible cracks on the surface and sides of the MLC. These cracks start at or near the termination and ceramic interface extending from the termination down along the MLC edge. This surface crack can become elliptical or circular shaped in the larger MLC sizes (1812 or larger). It is even seen in the 1210 size (120 mils x 100 mils) in very severe cases.

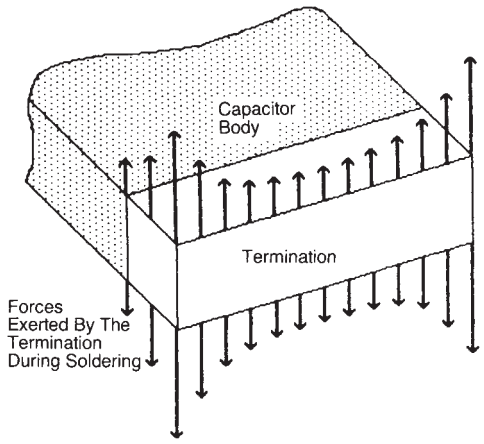

Figure 4. Stress Risers Caused by the Termination on the MLC Body

Figure 4 shows the stress risers generated by the termination on the ceramic body. Once a crack is initiated, it will propagate away from these stress risers giving rise to classical thermal shock cracks. Figures 5 and 6 show this physical manifestation of extreme thermal shock. Full elliptical surface cracks due to thermal shock are sometimes mistaken as damage caused by the pick and place machine bit smashing the MLC onto the substrate. If an MLC has been smashed or crushed, the surface crack will not be smooth but will have a rough or powdered edge. In fact it is quite difficult to cause surface cracks with pick and place machines, the parts being generally crushed or broken into pieces.

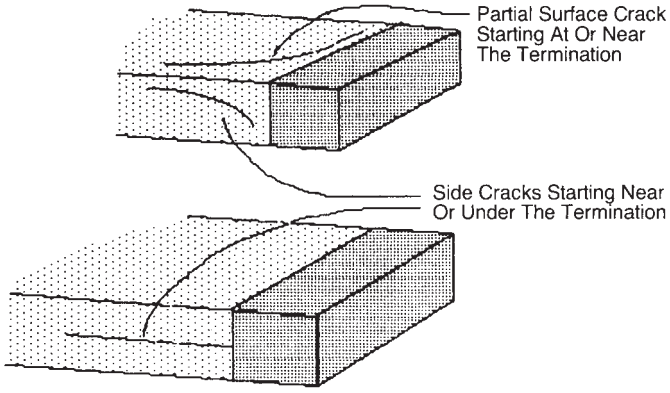

Figure 5. Extreme Thermal Shock Cracks in MLCs

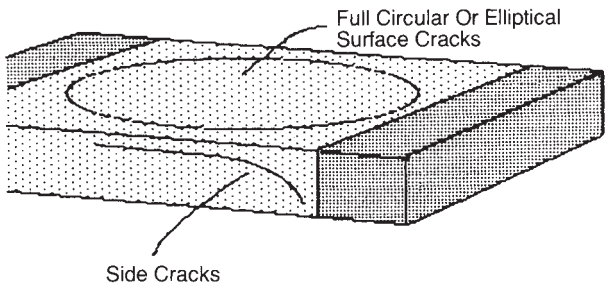

Figure 6. Severe Thermal Shock Cracks in Large MLCs

Thermal shock has two manifestations, obvious visible cracks and the more insidious, invisible micro crack. Micro cracks are formed at or just under the termination and ceramic interface along isothermal lines (constant temperature lines) at slower temperature rates of rise. Maximum shear occurs along these lines at the termination and ceramic interface during the fastest temperature increases of soldering.

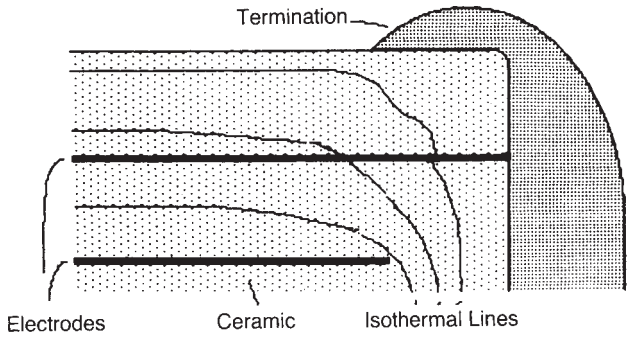

Figure 7. Isothermal Line Shortly After Exposure to Solder Temperatures

The micro crack will propagate along isothermal lines where the capacitor structure received maximum stress. This propagation takes a long time and is dependent on the physical size of the capacitor, CTE difference between the substrate and capacitor and actual temperature excursions during power cycling. Crack propagation is minimized with small components, small differences in CTE and low temperature swings, unfortunately the real world is not ideal and large differences do exist.

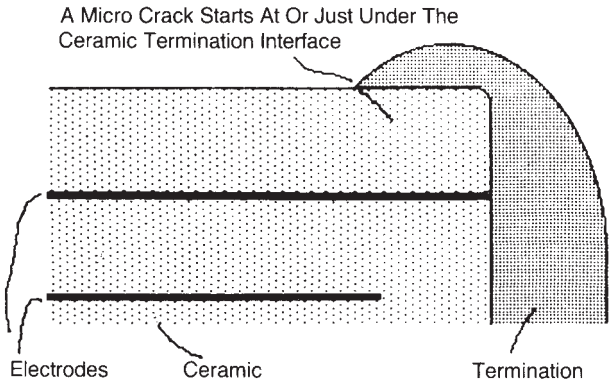

Figure 8. A Micro Crack at the Termination Ceramic Interface

Large CTE differences or physically large components[1] will have increased forces on the part during power cycling due to the linear displacement of size or CTE difference. When the substrate's CTE is larger than the component such as PC boards and MLCs, the part is held in tension during power cycling and micro cracks propagate more quickly than if they were in compression. When an MLC is mounted on

alumina the opposite is true (now compression) and the micro crack will propagate more slowly. (The reverse would be true for cooling cycles.)

MATERIAL	CTE (ppm/°C)
Alumina	≈7
Barium Titanate Capacitor Body	9.5-11.5
FR-4/G-10 PC Boards (X, Y)	≈18
Polyimide/Glass PCB (X, Y)	≈12
Polyimide/Kevlar PCB (X, Y)	≈7
Copper Clad Invar	6-7
Copper	17.6
Tin Lead Alloys	≈27

Table 1. CTEs of Typical Components and Substrates

Increased electrical and mechanical failures are not acceptable alternatives for increased density, automation and improved electrical performance. Once the problem is understood and controls are instituted, any soldering technique can be used reliably. Unfortunately, once a user has experienced problems with thermal shock, they tend to go overboard with ill-considered or irrelevant tests that only prove that they can indeed exceed the mechanical strength of the parts.

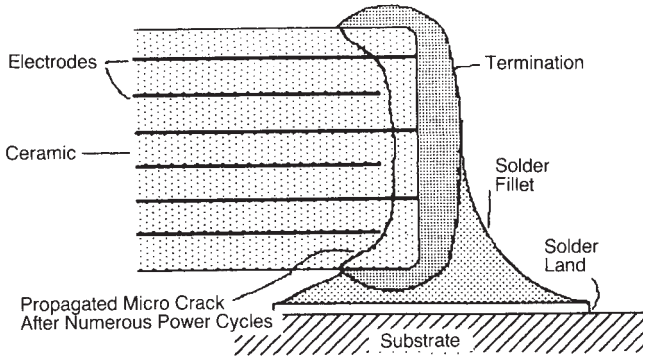

Figure 9. A Propagated Micro Crack After Power Cycling

These tests include plunging the part into a solder pot with tweezers with unknown pressure, position or size or they solder components to a test board with exaggerated solder temperatures. Different lots from different vendors might pass such tests but the main problem is that surface mount manufacturing requires process modification to insure reliable assemblies. In particular, wave soldering is the biggest problem because many manufacturing groups do not want to change solder temperatures or flux. They insist that the vendor must comply with a process that will not work reliably and will cause long term failures that show up many months later as field service problems. Remember all soldering processes must be component and material vendor independent.

Surface mount manufacturing requires discipline; a reliable process must be developed and adhered to, solder profiles run each shift and solderable components used. This will be a new experience for some manufacturing groups that use the "crank the temperature up" philosophy (remember if you crank it up field service must recrank it up).

The following process guidelines allow proper soldering with minimum thermal shock and component degradation with maximum yield.

WAVE SOLDER: This is the most critical process. The actual solder wave temperature should be reduced from 250°C-260°C to 232°C ±2°C for 60/40 solder and the preheat temperature of the assembly bottom should exceed 140°C with the rate of rise limited to 4°C/sec. The total wave dwell time for components should not exceed 10 seconds with 5-7 sec as an optimum time allowing adequate soldering with obtainable preheat temperatures. The higher the preheat or smaller difference between the preheat and solder wave temperature the better. The absolute maximum difference between preheat and solder wave should be less than 100°C, 70-80°C is a better number eliminating any possibility of micro cracks.

It's not uncommon to see solder wave temperatures exceeding 300°C with low or no preheat in "crank it up" manufacturing groups because the solder wave controls have gone into thermal run away. There is a fear of using high preheat in wave soldering because of low melting point plastics used in some thru hole components but only the board bottom is being heated. Actual measured thru hole component temperatures are well within any maximum limits. Some manufacturing groups are now using wave temperatures as low as 225°C with higher preheat to achieve zero soldering defects with sub ppm long term return rates. Simply stated they control the solder process to eliminate field returns.

VAPOR PHASE REFLOW SOLDERING: VPR soldering does not produce visible cracks but can cause micro cracks if improper preheat is used. A preheat of 100°C is recommended for VPR soldering. This will eliminate micro cracks while drying and activating the solder paste, improving soldering and minimizes solder balls or splatter. Component termination temperature rates of rise in excess of 50°C/sec have been measured when no preheat is used in a VPR system. These rates of rise will induce micro cracks because the component cannot heat uniformly or quickly even with the uniform heat source.

Dwell time in the saturated vapor zone needs to be less than one minute which yields excellent soldering with a minimum of solder migration. At longer dwell times, degradation of epoxy resin molded parts such as transistors, ICs, tantalum capacitors, etc., is accelerated due to these components maximum temperature capabilities and the epoxy resin's low glass transition temperature, T_g. This is the temperature where the long molecular chains in the resin become very active with CTE increasing from 18-25ppm/°C to over 200ppm/°C. T_g for most epoxies is in the 80 to 125°C range and over 200°C for polyimides. Some complex PC boards with

high thermal mass will require longer times in the vapor zone but care must be taken to absolutely minimize this time.

HOT BELT REFLOW AND IR REFLOW: Any thermal shock is unusual when IR reflow is used because of the lower heat transfer rate. The maximum temperature rate of rise should be less than 4°C/sec (1-2°C/sec typical) which allows uniform substrate heating and minimum stress on the components.

Hot belt reflow is used mainly for hybrids or assemblies on alumina substrates and can cause problems if high temperature solders such as goldgermanium are used because of very high temperature rates of rise due to short heat zones. A micro crack will form and propagate through the capacitor very quickly during rapid heat up and cool down and can actually pull the termination right off of the component. Temperature rates of rise should be limited to 4°C/sec maximum for hot belt reflow. Most surface mount assemblies use 63/37 eutectic solder or low silver bearing solder such as 62/36/2 which minimizes solder migration and termination leaching. These solders have melting points near 186°C. An ideal profile for IR or hot belt reflow with these solders will have a peak temperature of 215-219°C with 45-60 seconds above the melting point.

These guidelines allow reliable assemblies to be built. The multilayer ceramic capacitor is sensitive to thermal shock but all electronic components share this problem especially tantalum capacitors. Table 2 lists CTEs and δ_T for common materials used to make chip resistors, SOTs (small outline transistors), SOICs (small outline integrated circuits) and other epoxy resin molded components.

MATERIAL	CTE (ppm/°C)	δ_T (W/m°K)
Alloy 42	5.3	17.3
Alumina	≈7	34.6
Copper	17.6	390
Filled Epoxy (<T_g)	18-25	.5
Nickel	15	86
Silver	19.6	419
Steel	15	46.7
Tantalum	6.5	55
Tin Lead Alloys	≈27	34

Table 2. CTEs and δ_Ts of Component Materials

All surface mount components are built with different materials that expand and conduct heat at different rates. If a part is heated up too rapidly, it will crack or internal seals are lost so the part will fail more quickly because the stress cannot spread throughout the component body. Proper processing eliminates these problems but users and vendors must understand the component limitations and not exceed those limits.

Reference

1. B.S. Rawal, etc., "Factors Responsible for Thermal Shock Behavior of Chip Capacitors."

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