TECHNICAL PAPER

Reliability of MLCCs After Thermal Shock

Bharat S. Rawal
Michael Childs
Allan Cooper
Bill McLaughlin

KYOCERA AVX Components Corporation
17th Avenue South
P.O. Box 867
Myrtle Beach, SC 29577

Abstract

With increasing use of multilayer ceramic capacitors in surface mount applications, the understanding of thermal shock properties of these devices is becoming increasingly important. Of the various soldering techniques utilized in surface mount applications, including wave soldering, vapor phase and infra red reflow techniques, wave soldering imposes the most severe thermal stresses on the MLCs. To simulate this process, parts are often dipped in solder baths. It will be shown in this paper that properties like critical stress intensity factor K1C, thermal diffusivity, Young's modulus and the chip geometry are important for understanding the thermal shock behavior of chips. Examples of effects of K1C and chip geometry will be shown.

RELIABILITY OF MULTILAYER CERAMIC CAPACITORS AFTER THERMAL SHOCK

by Bharat S. Rawal
Michael Childs
Allan Cooper
Bill McLaughlin

I. Introduction

An earlier study by Rawal, Ladew and Garcia[1] clearly demonstrated that the mechanical and thermal shock resistance parameters of multilayer ceramic capacitors (MLCs) are important for understanding the surface mount applications of these devices. In particular, it was shown that thermal stresses resulting from rapid changes in temperature (for example, plunging MLCs in a solder bath) can explain the thermal shock properties of these capacitors. These thermal stresses σ_s can be defined by

$$\sigma_S = \frac{E\alpha}{1-\mu} \quad \frac{s\o t^2}{(k/\rho C_p)} \qquad (1)$$

where E is the elastic modulus, α is the coefficient of linear thermal expansion, s is the shape factor, ø is the rate of change of temperature, t is the thickness, μ is the Poisson's ratio and $(k/\rho C_p)$ is the thermal diffusivity with k, ρ an C_p being the thermal conductivity, density and specific heat respectively. As suggested by equation (1), experimental results[1] demonstrated that thermal shock behavior of chips can be dramatically improved by lowering rates of change of temperature and by utilizing thinner geometries of MLCs because thermal stresses have a square dependence on the thickness of chips. In addition, thermal stresses can be decreased by changing the surface heat transfer coefficient h implicit in the thermal diffusivity defined by $(k/\rho C_p)$ and thermal shock behavior can be improved by utilizing ceramic materials with higher fracture toughness, K_{1C}. The thermal stresses by themselves are not sufficient for failure to occur; crack initiation and crack propagation, and the corresponding thermal stress resistance parameters R' and R", play an important role in the thermal shock behavior of chips. Further evaluation of dielectric materials show[0] that parameters like the elastic moduli and thermal diffusivities show significant changes to effect thermal stresses and may be utilized to improve the thermal shock behavior of chips.

In this paper it will be shown that improvements achieved by changing the chip geometries, by utilizing materials with lower elastic moduli and higher thermal diffusivities and by optimizing K_{1C} values, the thermal shock behavior of chips can be dramatically improved. Examples of changes in the thermal shock behavior of chips with changes in the K_{1C} values and thickness of chips will be shown. Results of chips which have been optimized will then be presented to demonstrate the reliability of these chips as measured by standard dry life test and by 85ºC/85%RH testing. Concerns have also been raised about crack initiation sites from laser marking on the surfaces of chips; thermal shock, dry life and 85ºC/85%RH test results will be presented before and after laser marking of chips.

II. Experimental Procedure

A. Ceramics Evaluated

In an effort to understand the role of thermal and mechanical stresses and their effect on thermal shock behavior of chips, various experiments were carried out with dielectric compositions classified by EIA temperature characteristics as X7R and Z5U ceramics.

B. Thermal Stress Evaluation Test Method

The thermal stress resistance behavior of chips was studied by both the solder dip and the wave solder test techniques described in our earlier paper[1]. The solder dip test technique was modified to utilize a controlled speed of entry and exit of 100 in./min. with no preheat and the wave solder experiments were carried out with no preheat at 10 feet/minute with 60Sn/40Pb solder at 260ºC. These test conditions are considered severe for majority of the surface mount applications and the failure was defined by presence of any cracks during the visual examination of all six sides for the solder dip test or examination of five sides of the parts on the board for the wave solder test.

C. Evaluation in the Salt Water Solution

After the parts were subjected to the solder dip test or the wave solder immersion, they were placed in 1.3 N aqueous NaCl solution at room temperature. The salt water was brought to a boil for 1 hour ±3 minutes in a covered container which was then allowed to cool to room temperature without any forced air cooling. Parts were rinsed in deionized water several times, air dried, allowed to stabilize at room temperature for 24 hours and then evaluated for any change in the insulation resistance as compared to the initial IR readings.

D. Life and 85ºC/85%RH Testing

Parts were subjected to a regular dry life test at twice rated voltage for 1000 hours and for 85ºC/85%RH at twice rated voltage for up to 500 hours. The post IR must meet 10% of the initial requirements.

GROUP	CHIP STYLE	CAPACITANCE VALUE (µF)	COMMENTS FOR SAMPLE PREPARATION	CHIP THICKNESS (mm)	K_{1C} ($MPa.m^{1/2}$)	THERMAL SHOCK (NUMBER OF FAILURES TO TOTAL NUMBER TESTED)
(a)	1206	0.001	Ceramic A normally used	0.85	1.3	0/50
	1206	0.001	Ceramic B with significantly lower K_{1c}	0.85	0.9	37/50
(b)	1210	0.1	Ceramic A normally used	0.85	-	0/50
	1210	0.1	Ceramic A thickness increased to induce thermal shock	1.5	-	25/50

Table 1. Effect of K_{1C} and Thickness on Thermal Shock Behavior of X7R Chips with a Barrier Termination

III. Results and Discussion

A. Effect of K_{1C} and Thickness of Chips on Thermal Shock

In Table 1, thermal shock results are shown in group (a) for 1206 0.001µF X7R parts made from ceramic A with K_{1C} value of 1.3 $MPa.m^{1/2}$ and from ceramic B with K_{1C} value of 0.9 $MPa.m^{1/2}$ respectively. As the solder dip tests results in the last column clearly show, the susceptibility to thermal shock changes dramatically from parts with no failures to parts showing about 75% failure rate. This clearly demonstrates that the choice of the type of X7R dielectric with higher K_{1C} is very important.

Also shown in this table are results of 0.1 1210 X7R chips with 0.85 and 1.5mm thicknesses respectively. As expected from equation (1), the thermal stress increases by more than a factor of three for the thicker chips and the corresponding number of failures are zero for the thinner chips compared to roughly 50% failure rate for the thicker chips. This clearly demonstrates the importance of thickness in the design of these chips.

B. Effect of Thermal Shock and Salt Water Boil Testing

As pointed out in section (A) above, optimization of parameters like K_{1C}, thickness, thermal diffusivity and elastic modulus can be utilized to improve the thermal shock behavior of chips. Results of solder dip and wave solder testing of various 0805, 1206, 1210, 1812 and 1825 size chips optimized for improved thermal shock behavior are shown in Table 2. These wave solder experiments were carried out with no preheat at 10 feet/minute on a single wave wave-solder machine[3] and no failures as characterized by visual cracking were observed. The solder dip experiments show isolated failures and these are ascribed to parts getting uneven heating or difficulty in controlling the solder dip experiment itself where no preheat is used. These experiments are more severe for the rate of change of temperature on the part which in turn results in higher σ_s, and therefore isolated failures. It is interesting to note that the salt water boil test picks up the same failures characterized as failures by visual cracks and by degradation of IR of parts after boiling in the salt water solution; no additional failures are observed. This result clearly demonstrates that visual observation is an effective first order approach for evaluating thermal shock failures of parts.

STYLE	MFD VALUE	SAMPLE SIZE	NUMBER OF FAILURES WAVE	DIP	NaCl H_2O
0805	.001	55	0	0	0
0805	.01	55	0	0	0
0805	.01	55	0	0	0
0805	.022	55	0	0	0
1206	.001	55	0	0	0
1206	.01	55	0	0	0
1206	.01	55	0	0	0
1206	.022	55	0	0	0
1206	.047	55	0	0	0
1206	.047	55	0	0	0
1206	.047	55	0	0	0
1206	.1	55	0	0	0
1206	.1	55	0	1*	1*
1210	.01	55	0	0	0
1210	.027	55	0	0	0
1210	.047	55	0	0	0
1210	.1	55	0	0	0
1210	.1	55	0	0	0
1210	.1	55	0	0	0
1210	.1	55	0	0	0
1210	.1	55	0	1*	1*
1812	.18	55	0	0	0
1812	.22	55	0	0	0
1812	.22	55	0	1*	1*
1825	.47	55	0	0	0
1825	.47	55	0	2*	2*
TOTALS		1375	0	5	5

* same unit

Table 2. Effect of Thermal Shock and Testing with 1.3 N Salt Water Solution Boil

C. Life and 85ºC/85%RH Test Results

In Table 3, results are shown for regular dry life testing of various 0805, 1206, 1210, 1812 and 1825 parts at twice rated voltage, 125ºC after they are subjected to the solder dip test. Parts exhibiting low IR, if any, after the salt water boil test were excluded from the life test. As these results clearly show, the parts which do not exhibit low IR after the salt water test show excellent reliability. As summarized in Table 4, after roughly six-and-half million unit hours, the failure rate is 0.036% per 1000 hours at twice the rated voltage, 125ºC at 90% confidence level which translates to 0.56 FITS at 50ºC and half-the-rated voltage simulating actual use conditions.

Various groups tested in Table 3 were subjected to 85ºC/85%RH testing and the results are listed in Table 5. Once again, over a wide range of part sizes and part values the results clearly demonstrate that the failure rates are

STYLE	MFD VALUE	SAMPLE SIZE	NUMBER OF FAILURES
0805	.001	30	0
0805	.022	30	0
1206	.001	29	0
1206	.0015	30	0
1206	.01	30	0
1206	.012	30	0
1206	.022	30	0
1206	.022	30	0
1206	.047	29	0
1206	.047	30	0
1206	.1	30	0
1206	.1	30	0
1210	.1	30	0
1210	.1	30	0
1210	.1	30	0
1210	.1	30	0
1210	.1	30	0
1210	.1	28	0
1210	.1	30	0
1812	.18	30	0
1812	.22	30	0
1812	.22	30	0
1812	.22	29	0
1812	.22	30	0
1825	.47	29	0
1825	.47	30	0
1825	.47	30	0

Table 3. Life Test Results of X7R Parts After Thermal Shock

STYLE	TOTAL UNIT HOURS	SAMPLE SIZE	NUMBER OF FAILURES	%/1000 HOURS
0805	48,000	60	0	0.48
1206	2,482,283	298	0	0.094
1210	1,777,616	208	0	0.13
1812	1,250,296	149	0	0.185
1825	538,705	89	0	0.43
TOTAL	6,528,900	804	0	0.036

Table 4. Summary of Life Test Results of X7R Parts at 90% Confidence Level After Thermal Shock

extremely low considering that these parts have been subjected to severe thermal shock testing where parts are dipped in solder with no preheat. The failure rate is less than a few FITS at the use conditions mentioned above; actual number is difficult to calculate because acceleration factors in the humid environmental testing are still being determined[4].

D. Laser Marked Parts

1. Solder Dip Results

In Table 6, solder dip test results of laser marked and unmarked X7R and Z5U parts made with varying K_{1C} or unusually thick chips are shown. The results clearly demonstrate that there are no significant differences between marked and unmarked parts.

2. Life Test Results

Laser marked parts from groups shown in Table 3 subjected to solder dip tests were subsequently life tested at twice rated voltage, 125ºC and the results are shown in Table 7. Once again, no degradation of IR or failures are observed clearly demonstrating that marked surfaces on the chips are not acting as crack initiation sites.

STYLE	MFD VALUE	SAMPLE SIZE	NUMBER OF FAILURES
1206	.001	20	0
1206	.001	20	0
1206	.01	20	0
1206	.047	20	0
1206	.047	20	0
1206	.1	20	1
1206	.1	20	0
1206	.1	20	0
1206	.1	17	0
1210	.047	20	0
1210	.1	20	0
1210	.1	20	0
1210	.1	20	0
1210	.1	19	0
1210	.1	20	0
1210	.1	20	0
1210	.1	20	0
1210	.1	20	0
1210	.15	19	0
1812	.033	20	0
1812	.18	20	1
1812	.22	20	0
1812	.22	20	0
1812	.22	20	0
1812	.22	19	0
1825	.47	20	0
1825	.47	20	0

Table 5. 85ºC/85%RH Test Results of X7R Parts After Thermal Shock

CHIP STYLE	CAP VALUE (µF)	COMMENTS FOR SAMPLE PREPARATION	THERMAL SHOCK	
			MARKED	UNMARKED
1206	0.001	Ceramic A normally used	0/50	0/50
1206	0.001	Ceramic B with significantly lower K_{1C}	37/50	35/50
1210	0.1	Thickness increased to induce thermal shock	2/50	1/50
1210	0.33	Thick Z5U Units	6/50	5/50
1210	0.068	Thick Units	2/50	2/50
1808	0.1	Thick Units	1/50	2/50

Table 6. Thermal Shock of Laser Marked vs. Unmarked X7R and Z5U

STYLE	MFD VALUE	SAMPLE SIZE	NUMBER OF FAILURES
1206	.0068	30	0
1206	.01	30	0
1206	.01	30	0
1206	.012	30	0
1210	.047	24	0
1210	.068	30	0
1210	.1	28	0
1210	.1	30	0
1210	.1	30	0
1210	.15	30	0
1812	.1	30	0
1812	.18	30	0

Table 7. Life Test Results of Laser Marked Parts Subjected to Solder Dip Tests

STYLE	MFD VALUE	SAMPLE SIZE	NUMBER OF FAILURES
1206	.047	20	0
1206	.1	20	0
1210	.047	20	0
1210	.1	20	0
1210	.1	20	0
1210	.1	19	0
1210	.1	20	0
1210	.15	20	0
1812	.1	20	0
1812	.18	20	1

Table 8. 85ºC/85%RH Test Results of Laser Marked Parts Subjected to Solder Dip Test

3. 85ºC/85%RH Testing

Parts subjected to regular life tests were also tested at 85ºC/85%RH at 100 volts and as shown by the results in Table 8, the failure rates are once again very low suggesting that the laser marked surfaces are not acting either as crack initiation sites or as sites where the cracks propagate and form a conducting path in these devices.

IV. Conclusions

1. It has been clearly demonstrated that materials properties like K_{1C}, thermal diffusivity and elastic modulus, and the thickness of multilayer ceramic capacitors play a key role in the design of these devices.

2. These parameters can be optimized to develop MLCs with very low failure rates as characterized by dry life test and 85ºC/85%RH testing.

3. Laser marked and unmarked parts show similar failure rates with the solder dip testing for thermal shock.

4. Laser marked surface does not act as a crack initiation or a crack propagation site, and both life test and 85ºC/85%RH test results show very low failure rates which are comparable to unmarked parts.

References

(1) Bharat S. Rawal, Richard Ladew and Ricardo Garcia, "Factors Responsible for Thermal Shock Behavior of Chip Capacitors," Proceedings of the Electronic Components Conference, 1987, pp. 145-156.

(2) G.S. White, C. Nguyen and B. Rawal, "Young's Modulus and Thermal Diffusivity Measurements of Barium Titanate Based Dielectric Ceramics," in Proceedings of Nondestructive Testing of High Performance Ceramics, 1987, pp. 371-379.

(3) Wave Solder Machine used was Hollis Model #282691.

(4) B.S. Rawal et al., "Thermal Shock and Reliability of Parts in Various Humid Conditions," to be presented at the ECC Meeting, 1989.

NORTH AMERICA
Tel: +1 864-967-2150

ASIA
Tel: +65 6286-7555

CENTRAL AMERICA
Tel: +55 11-46881960

EUROPE
Tel: +44 1276-697000

JAPAN
Tel: +81 740-321250

NOTICE: Specifications are subject to change without notice. Contact your nearest KYOCERA AVX Sales Office for the latest specifications. All statements, information and data given herein are believed to be accurate and reliable, but are presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements or suggestions concerning possible use of our products are made without representation or warranty that any such use is free of patent infringement and are not recommendations to infringe any patent. The user should not assume that all safety measures are indicated or that other measures may not be required. Specifications are typical and may not apply to all applications.