TECHNICAL PAPER

Capacitor Selection and EMI Filtering

Jeffrey Cain and Steve Makl
KYOCERA AVX Components Corporation
Myrtle Beach, SC

Abstract
MLCCs are an inexpensive, yet effective, method for reducing the noise on both power/ground systems and signal lines themselves. Choosing the proper capacitance value such that the impedance is minimized at the frequency of interest also makes a difference.

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CAPACITOR SELECTION AND EMI FILTERING

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Introduction

Bypass and decoupling capacitors have long been used to reduce the amount of noise generated on printed circuit boards (PCBs). Due to their relatively low cost, availability and wide range of values, capacitors are often the main devices utilized to reduce electromagnetic interference (EMI) at the circuit board level. The selection of the proper capacitor involves more than just a choice of the capacitance value, as parasitics play an important role. There are many ways to build capacitors, and their construction determines the magnitude of the parasitics.

Electrical noise can be caused in a number of different ways. In the digital environment, this noise is mainly generated by the switching integrated circuits, power supplies and regulators. RF circuits can also be susceptible to noise generated in oscillator and amplifier circuitry. Whether on the power and ground planes or the signal lines themselves, this interference can wreak havoc with the operation of the system, as well as cause radiated emissions.

This article deals with multilayer ceramic capacitors, both surface-mount and leaded. The correlation between impedance and insertion loss for these simple devices are calculated. Modified formats, such as feedthrough and low inductance, are measured and equivalent circuit models are shown. These models are derived from measured data and the measurement techniques are shown. These parasitics are examined for all of the different constructions and the resulting impedance curves are given.

Impedance and Insertion Loss

Fortunately, capacitors are relatively simple devices. There is only one way to shunt a capacitor across a transmission line, since it is a two-terminal device. Instead of thinking of the device as a capacitor, it is easier to consider it a block of impedance. When it is shunted across the transmission line, one could even consider the block an admittance (Figure 1).

The ABCD parameters for this particular connection can be as shown as:

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ Z^{-1} & 1 \end{pmatrix} \quad (1)$$

Then using the relationship between ABCD parameters and scattering (S) parameters, one can find that the magnitude of the insertion loss, S_{21}, is:

$$|S_{21}| = 20 \log\left(\frac{2|Z|}{\sqrt{4|Z|^2 + Z_0^2 + 4|Z|Z_0\cos\theta_Z}}\right) \quad (2)$$

where
$|Z|$ = magnitude of the impedance
Z_0 = impedance of the transmission line
θ_Z = phase angle of the impedance block

There are some interesting points to look at when one examines Equation (2). First, the phase angle for a good ceramic capacitor is very near ±90° for almost the entire frequency spectrum, except near the resonance point (Figure 2).

Knowing that the cosine is nearly zero, Equation (2) can be simplified to

$$|S_{21}| = 20 \log\left(\frac{2|Z|}{\sqrt{4|Z|^2 + Z_0^2}}\right) \quad (3)$$

so that the phase can be ignored and still give good results for most of the frequency spectrum. Another approximation that holds very well is for $Z_0 >> |Z|$. This further simplifies Equation (3) to

$$|S_{21}| = 20 \log\left(\frac{2|Z|}{Z_0}\right) \quad (4)$$

As an example, the measured impedance and calculated insertion loss for a 1000-pF bypass capacitor are shown (Table 1). All the insertion loss data is referenced around 50 ohms. As this table shows, Equation (3) breaks down rather quickly once the impedance of the capacitor begins to increase to 50 ohms.

The only problem with these equations is that one needs to know the impedance for a wide range of capacitance values. The next section will cover the models and measurement techniques needed to compute the impedance.

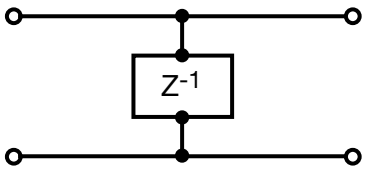

Figure 1. Capacitor as Block of Admittance.

Multilayer Ceramic Capacitors (MLCC) Series Model

The simplest (and arguably most effective) model that can be used for an MLCC chip is the series model (Figure 3).

This model gives the correct impedance curve for almost any surface-mountable MLCC that can be constructed. Keep in mind that the capacitance varies with temperature and dc bias. The equivalent series

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resistance (ESR) varies with temperature, dc bias and frequency, while the equivalent series inductance (ESL) remains fairly constant. Perhaps the most important part of the impedance is the resonant point, as this will be the frequency that is attenuated the greatest. The well-known formula for the resonant frequency is:

$$f_r = \left(\frac{1}{2\pi\sqrt{C \cdot ESL}} \right) \quad (5)$$

Inductance values for a wide range of surface-mount packages calculated with the measurement technique described in Equation (2) are available. As an example, if the system is generating 800-MHz noise, then this interference can be traced to a certain part of the PCB. Choosing a package with a standard capacitance value of 39 pF and placing it as close as possible to the noise generator would be the best choice to reduce the EMI.

An effective way to lower the inductance of a rectangular chip is to modify the design to terminate the chip longways. The impedance curves for selected capacitors are shown (Figure 4). Note that by changing the aspect ratio, the parasitic inductance is lowered by approximately 50 percent, from 1200 pH to 600 pH. This effectively shifts the maximum attenuation point, so one must keep that in mind when attempting to use these chips for EMI filtering.

The greatest advantage of the low inductance capacitor is in digital decoupling. Using the simple inductance equation

$$v = L\frac{di}{dt} \quad (6)$$

Using low inductance chips to lower the inductance, the amount of voltage noise created when the integrated circuits are switching can be reduced.

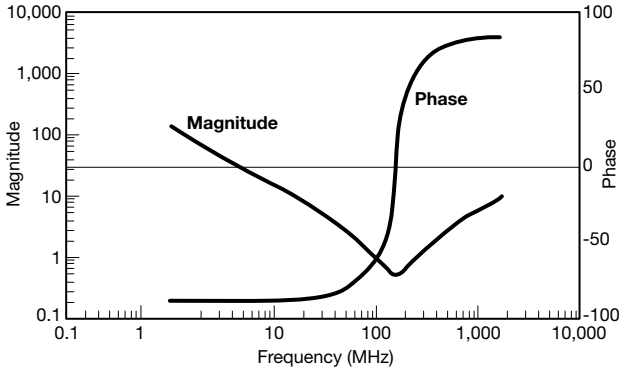

Figure 2. Typical Impedance Magnitude and Phase for a 1000-pF Ceramic Capacitor.

Frequency	Impedance (W)	S_{21} (2) (dB)	S_{21} (4) (dB)
1 MHz	159.0	-0.12	16.10
10 MHz	15.9	-5.60	-3.93
100 MHz	1.1	-27.30	-27.13
1 GHz	6.1	-12.70	-12.20

Table 1. Impedance and Calculated Insertion Loss for a 1000-pF Bypass Capacitor.

Figure 3. Equivalent Series Model for a Ceramic Capacitor.

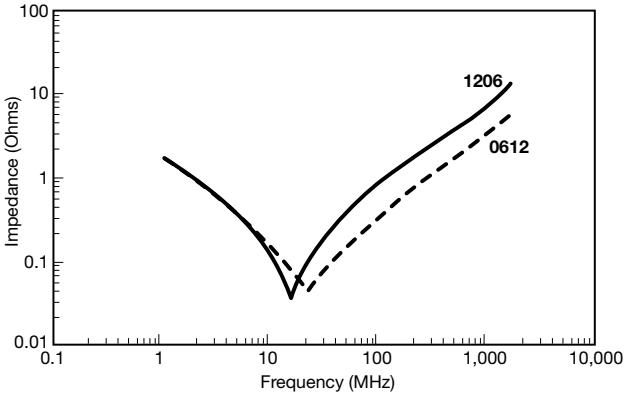

Figure 4. Impedance Curve Comparison for Two 0.1 µF Capacitors.

Leaded Capacitors

Leaded capacitors are nothing but surface-mount devices that have leads attached. The equivalent model is identical to the MLCC model with the exception of the added inductance from the leads (Figure 5).

Figure 5. Model for Leaded Capacitors.

The effects of lead inductance on the impedance are shown (Figure 6). A good rule of thumb is 2.5 nH of inductance for every 0.10" of lead length above the surface of the board. Just as the low inductance capacitors shift the frequency higher, leaded devices shift the frequency lower. For optimal EMI filtering this must be kept in mind.

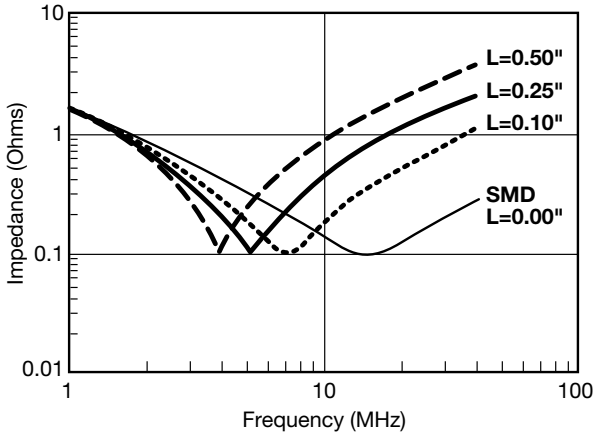

Figure 6. Lead Length Effects on 0.1 µF Capacitor.

Feedthrough Capacitors

The next improved level of EMI protection is the feedthrough capacitor chip. This is a three-terminal surface-mount device, as opposed to the two-terminal capacitor. The equivalent circuit for a feedthrough is shown (Figure 7). This configuration allows the signal to be fed through the device, with the capacitance filtering EMI noise to ground.

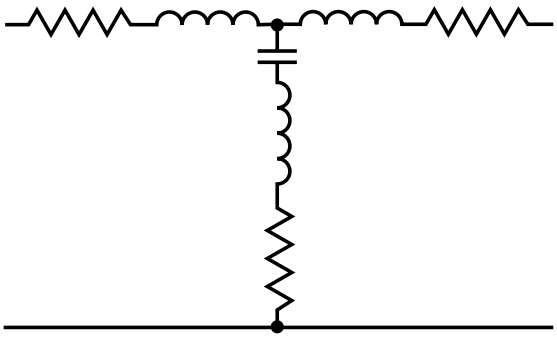

Figure 7. Feedthrough Capacitor Equivalent Circuit.

A couple of interesting things happen to the parasitics with this type of geometry. First, the parasitic inductance of the capacitor becomes much smaller than that for a similar sized chip with an equivalent capacitance. The parasitic inductance for the feedthrough can be measured to be 250 pH. The same phenomena that lowers the inductance also lowers the ESR (path length, path length, path length!). Lastly, the introduction of the inductance in the through section will increase the bandwidth of the attenuation. The insertion loss comparison between a 100 pF feedthrough and an equivalent standard chip capacitor is shown (Figure 8).

The surface-mount devices discussed here are related directly to the traditional bulkhead-mounted feedthrough filters which use discoidal capacitors. The equivalent circuit for this filter is similar to the feedthrough chip, but the shape of the discoidal leads to an even lower parasitic inductance. The filter is utilized on signal or power lines passing through a chassis or enclosure to attenuate both incoming and outgoing noise. When high frequencies (>500 MHz) are generated within a system, discoidal feedthroughs can be used to separate different systems (e.g., analog and digital) to remove unwanted interference.

However, even the best filtering scheme will not overcome poor circuit board layout. Connecting the capacitors by long, highly inductive traces will certainly affect the resonant point of the MLCC. If all the noise over the entire frequency spectrum is shunted to the ground plane and that plane acts like an antenna, then there will be high radiated emissions. Multilayer boards should be used whenever possible, with large power/ground planes embedded to lower the EMI generated by the system.

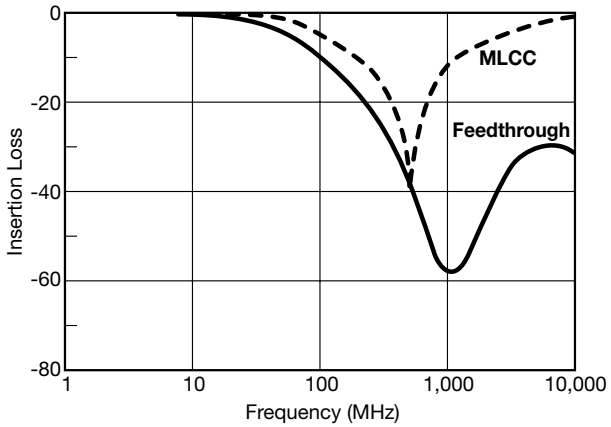

Figure 8. Comparison Between 100-pF Feedthrough and 100-pF Series Model Two-Terminal MLCC.

NORTH AMERICA
Tel: +1 864-967-2150

ASIA
Tel: +65 6286-7555

CENTRAL AMERICA
Tel: +55 11-46881960

EUROPE
Tel: +44 1276-697000

JAPAN
Tel: +81 740-321250