TECHNICAL PAPER

The Frequency Response Effects of Internal Component Con iguration on Multiple Ceramic Dielectric System

S. Pala
Czech Republic s.r.o., Dvorakova 328, 563 01 Lanskroun, Czech Republic

R. Demcko and M. Berolini

KYOCERA AVX Components Corporation
801 17th Ave. S; Myrtle Beach, South Carolina, USA

Abstract

The purpose of this paper is to discuss the frequency response effects of internal designs within ceramic systems. Those effects will be related to component performance parameters for devices used to suppress ESD and control EMI in high speed data lines, which are prone to be damaged by ESD. As communication speed increase, systems become more complicated and performance standards tighten, options to improve EMI/RFI performance becomes of great importance. Long term EMI performance and reliability are of particular importance in automotive, medical and aviation application sectors. A performance comparison will be made between single element traditional MLCC and MLV SMT devices. A second comparison will be made between 3 terminal MLCC filters and 3 terminal MLV filters using doped ZnO dielectrics. Internal designs to expand the MLVs frequency response (to higher and lower frequencies) will be presented. These range from lumping MLV/MLCCs in a single package to expand MLV frequency response to the use of non overlap electrodes to minimize internal device capacitance. The impact of sub pf MLVs will be shown through the use of eye diagrams.

KYOCERA AVX

Introduction

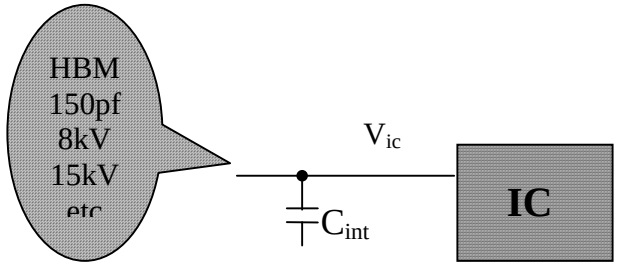
A common problem within any design is that of ESD and EMI control. Solutions to this complex problem are greatly affected by the internal electrode and ceramic configuration within a passive component.

One way to see the real world impact of internal component configuration is to compare an MLCC to a MLV in the complex performance requirements demanded for EMI and transient suppression.

Integration Capacitor:

Control of transient voltages and EMI can be achieved (to various levels) through the utilization of integration capacitors or transient voltage suppressors such as Multilayer Varistors (MLVs). Each method has its own set of advantages and disadvantages.

MLCC capacitors used as a transient integration capacitor are inexpensive, come in various case sizes and values to allow for a wide frequency range of EMI filtering. However, their use can have severe performance limitations.
First, the capacitor doesn't actually clamp anything; it shares the transient charge by dividing the voltage from the source and itself proportional to conservation of charge rules.
Using the conservation of charge rule to predict the resulting voltage after the integration capacitor requires an understanding of the equivalent model used to represent the incoming transients' characteristics. Commonly a capacitance, resistance and voltage are used to describe waveforms such as Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM) etc. Once the transient waveforms equivalent model is known and the integration capacitors value has been chosen the relative level of protection provided by the integration capacitor can be predicted according to the equation in figure 1.



$$C_{driver} * V_{driver} = C_{total} * V_{ic}$$

Where:
Cdriver = capacitance of the incoming transients model
Vdriver = voltage of the incoming transient
Cint = the value of integration capacitor
Ctotal = Cdriver + the value of the integration capacitor
Vic = Solve for Vic the voltage after the integration capacitor at the IC

Fig.1. Integration Capacitor Voltage resulting voltage - conservation of charge rule

What is important to note is that the integration capacitors value will drop dramatically during the incoming transient event as a result of the dielectrics voltage coefficient. That means the voltage expected based upon calculations of figure 1 is actually a best-case scenario. Further, the amount of capacitance drop varies by manufacturer, ceramic type and thickness and the speed and magnitude of the applied transient pulse. It is not impossible to experience a 70% (or larger) decrease in capacitance value as a result of the transient voltage bias. If we compound that transient capacitance variation with temperature related decrease we can

experience as 150° is approached (automotive under hood application for example) it is not inconceivable to have a 80% or 90% drop in capacitance from purchased values during an ESD event.

As an example, if an 8kv ESD strike were injected to the trace of a PCB utilizing a 100pF integration capacitor the best case transient voltage the IC would be subjected to would be 4.8kv assuming 100% transfer of charge of the ESD pulse to the PCB, zero transmission line effects from the circuit trace and zero variation of integration capacitors value during the pulse or temperature range. In the real world 100% coupling doesn't always occur and traces will act as a transmission line. There is no way to give an accurate generalization on the exact voltage at the IC without measuring or modelling for each specific PCB design, waveform type, capacitance value and capacitance manufacturer.

Multilayer Varistor (MLV)

Unlike MLCC integration capacitors, MLVs actually clamp transients in the on state and act as an EMI filter in the off state. MLVs are available in case sizes of 0201 and larger, are RoHS compliant and available through many different manufacturers. Therefore, MLVs are a very efficient, high reliability, low risk solution to fight transients.

The MLV consists of layers of doped zinc oxide (Zn0) separated by metallic electrodes and, in fact, look identical in construction to a chip ceramic capacitor. When the device is fired at high temperature, a diffusion of the dopants occurs and every grain of ceramic (millions, even in the smallest chip) is converted into a Schottky junction, i.e., the MLV becomes a mass of P-N junctions all packed into a series/parallel configuration [1].
When transient strike occurs, all of these "ceramic diodes" go into conduction and dissipate energy, which is why the energy density of MLV's is so high when compared to single junction, diode based products.
Without the transient strike, the MLV will act fairly similar to X7R MLCC in terms of temperature stability.

MLVs are designed in a fashion similar to a multilayer capacitor – see figure 2. Alternate electrodes are separated by a zinc oxide dielectric. Rather than using a traditional barium titinate dielectric, zinc oxide is used. The Zinc Oxide is doped with bismuth, cobalt, manganese and/or other metal oxides to obtain a bi-directional varistor effect. Regardless of the exact composition, the resulting grains are fired in a manner to yield similar sized grains whose numbers are equally spaced between the counter electrodes.

Perhaps the most important element of design within the MLV is its electrode system.
The electrode area and number of electrodes impacts the energy rating, in rush current rating and EMI filter response of the MLV. The conductivity of the electrode and its connection to the MLVs terminations (as well as the termination type) also effects the energy rating, in rush current rating and EMI filter response of the MLV.

Increased electrode area is an improvement that multilayer construction offers resulting in increased transient energy dissipation and more efficient current distribution within the suppressor. This allows smaller parts to be built. MLV design allows current and energy dissipation is uniformly distributed within the ceramic volume between electrodes. Additionally the multilayer structure has the added advantage of peripheral electrode current injection similar to high current power transistors. Not only is electrode area important for high current suppressors but electrode periphery is also important for maximum performance.

Simplified MLV Electrode Cross Section

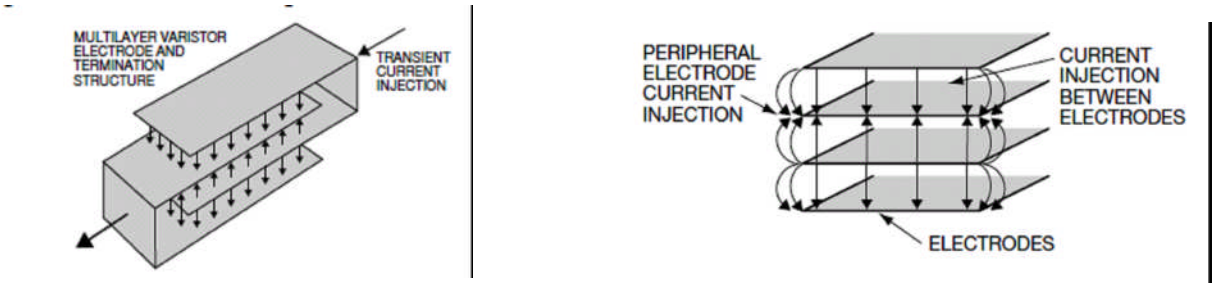


Fig.2. MLV construction

The frequency response effects of internal component configuration on multiple ceramic dielectric system

A self resonant frequency response comparison between common integration capacitors and MLV options was performed. In this exercise, the minimum to maximum capacitance values available in MLCC and MLV case sizes from 0201 to 1210 were tested and plotted in a case size by case size manner(see figure 3a and 3b).
The data shows that MLCC integration capacitors offer an excellent low frequency response. The data also shows MLCCs are somewhat limited in high frequency response. Low value MLCCs work fine as EMI capacitors but they are not effective at transient suppression.
Low value MLCCs integrate the transient voltage to a much lesser extent and therefore allow potentially damaging transients onto the IC.
It is for that reason that integration capacitors tend to be ineffective on high speed data lines. As capacitance value is decreased (in order not to destroy data) the effectiveness as a transient voltage control solution diminishes.
The effectiveness of an integration capacitor is limited though perfectly acceptable for extreme cost sensitive applications where extremely infrequent transients associated high series inductance exist.

The limitation to the MLV is its capacitance range. Common industry ranges for discrete devices range from < 1 pf to 20 nf. The advantage to the MLV is that it actually clamps the incident transient voltage in accordance to a VI curve. That VI characteristic can be built into virtually any case size and electrode configuration imaginable.
Therefore MLVs can be chosen for optimized case size, clamping and frequency response. Further improvements in noise attenuation and effective EMI filter response are expected by modifications to the configuration of the MLV.

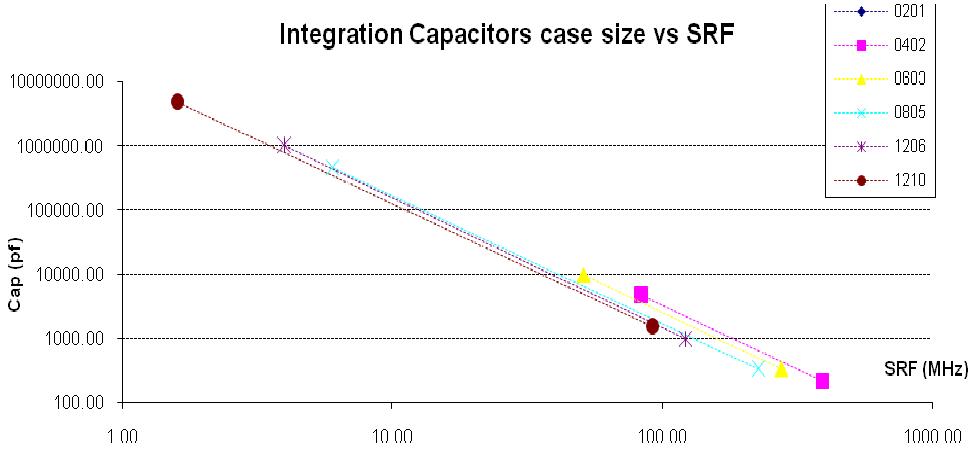


Fig.3a) Common Integration Capacitor SRF by case size

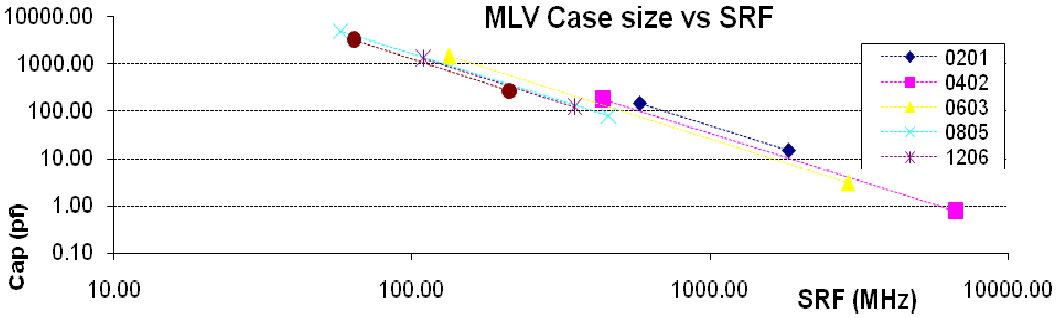


Fig.3b) Common MLV SRF by case size

Feedthru Filter Configuration

One method to further modify the frequency response of a MLV is to reconfigure it into a 3 terminal FeedThru device. When a MLV is configured in a 3 terminal fashion, it roughly looks similar to a T configured filter. Parallel inductance is dropped to <0.5 nh, resistance is dropped and the MLV turn reduces turn on time to < 250 ps.

A comparison of the forward transmission characteristics between a standard configured MLV and an MLV Feedthru shows that MLV FeedThru devices exhibit a higher frequency response and a deeper maximum attenuation number. This performance is expected and predictable based upon elimination of parasitic within a standard package. Parasitc loss reduction followed that of MLCC FeedThruogh designs. It is further expected that vertical electrode configurations produce further reductions in parasitic and improvements in turn on times.
MLV FeedThrus can be especially effective when chosen for maximum attenuation at RF spectrums corresponding to strictest emissions standards. (see Figure 4)

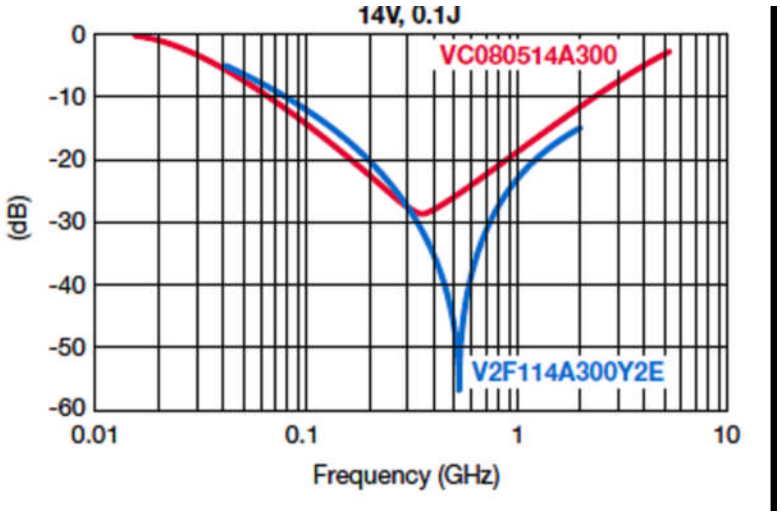


Fig.4. MLV configuration Comparison

A study similar to the self resonant frequency response comparison between common integration capacitors and MLV options was performed. In this case, the attenuation and SRF of SMT FeedThroughs was compared to MLV FeedThroughs and plotted across frequency, showing the capacitance loading for each filter type (see figure 5).

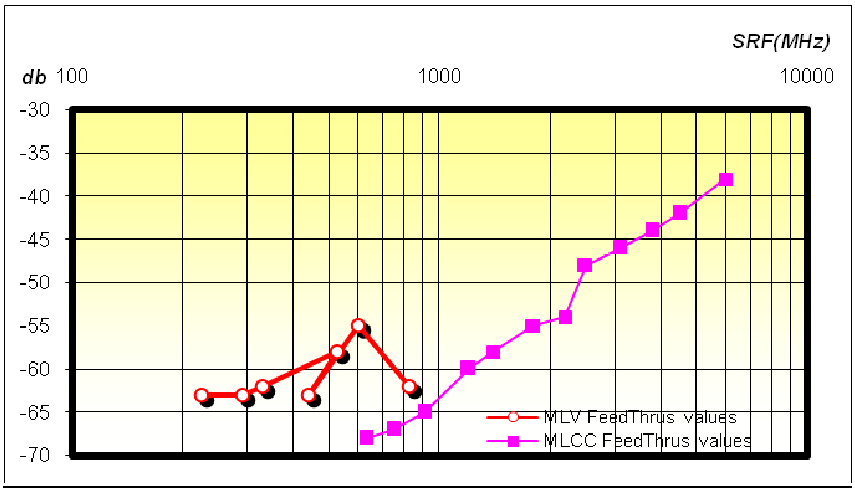


Fig.5. FeedThrough Filter attenuation comparison

FeedThrough Capacitors are available in larger values but were not included in this study. Further PI configured MLVs were not included in this study.

Methods to further broaden the filtering spectrum and magnitude of attenuation were investigated.

Stacked MLV MLCC solution

Low Frequency filter response of MLVs is easily addressed with the use of a parallel external MLCC to the MLV. In this configuration the MLCC and MLV are stacked upon one another and terminations soldered to form a single device. The values of capacitance are limitless and can easily create an enhanced low frequency EMI filter with a transient response.
Stacked packages first appeared with the introduction of stacked capacitors and have gained increased usage because of several technical advantages.
Among them are:

1) Stacked devices board space foot print efficiency – commonly XY board space is at a premium. Though component height above the PCB is important it is not nearly as dear as x y board area.

2) Reduced solder joints improve system reliability. Stacked passives use a high temperature solder under controlled thermal environments to join components.

3) Potential Improved ability to withstand harsh environment/ operational extreme exposure. In many cases stacked components are available in through hole DIP configuration as well as J, gull and various other lead frame configurations that optimize harsh environment performance.

An example of a common 12 nf MLCC in parallel with an 18v MLV is shown in Figure 6 below. The graph shows the broad frequency response attained with a stacked MLCC MLV combinations.

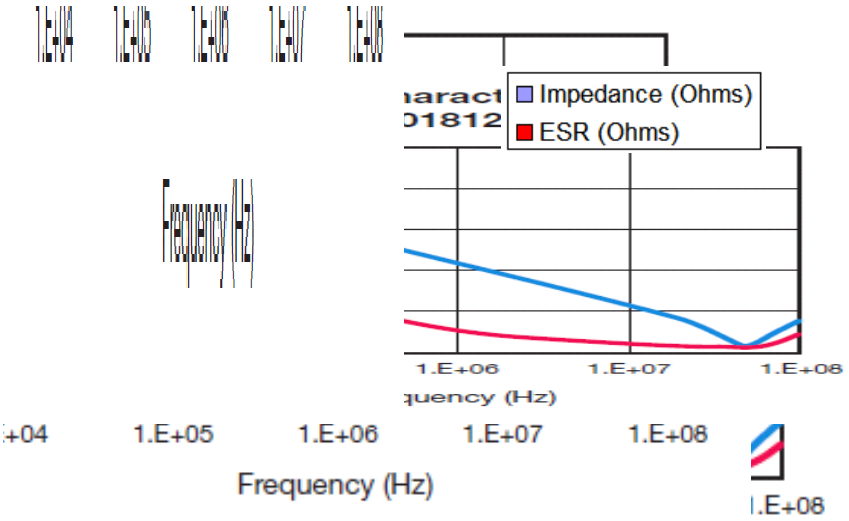


Fig.6. Stacked MLV MLCC Combination Impedance (ESR) vs Frequency

Minimal Electrode Overlap solutions
The importance of extremely low capacitance value suppressors cannot be overstated when it comes to the protection of high speed data lines. Options for reduced capacitance range from electrodes with no overlap to non traditional dielectrics and designs resembling spark gap designs. Capacitance value ranges as low as 0.05 pf can be offered using a combination of these methods.

Sub pf evaluation method – Eye Diagram

Eye diagrams are the preferred characterization method for component benchmarking given such low capacitances.

A common set up for eye diagram testing is to use a random bit-stream provided by a Tektronix® DTGM5334 signal mainframe with a DTG30 signal generator (see figure 7a). Eye diagrams were recorded on a Tektronix® DPO70804 digital phosphor oscilloscope using RT-Eye® software.
Parasitic control is critical. In this study the test board is a coplanar waveguide with SMA connectors and a total combined capacitance of 3.1pF (see figure 7b).

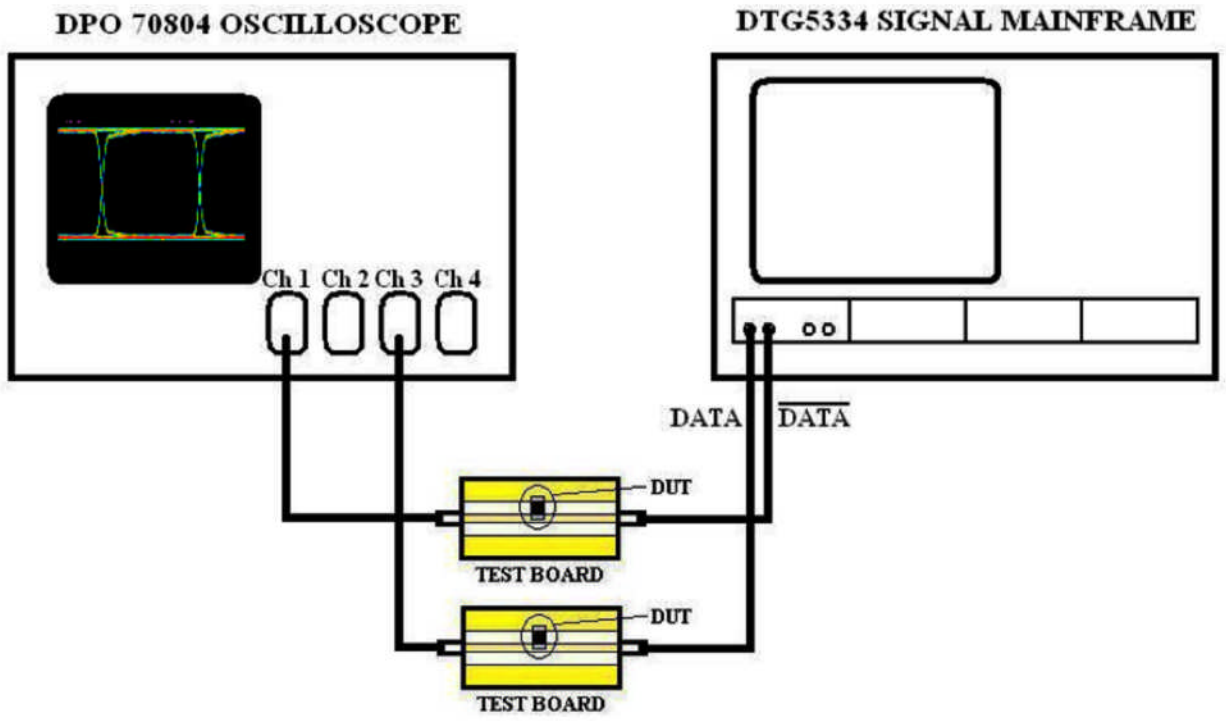


Fig. 7a) Eye Diagram Equipment set up

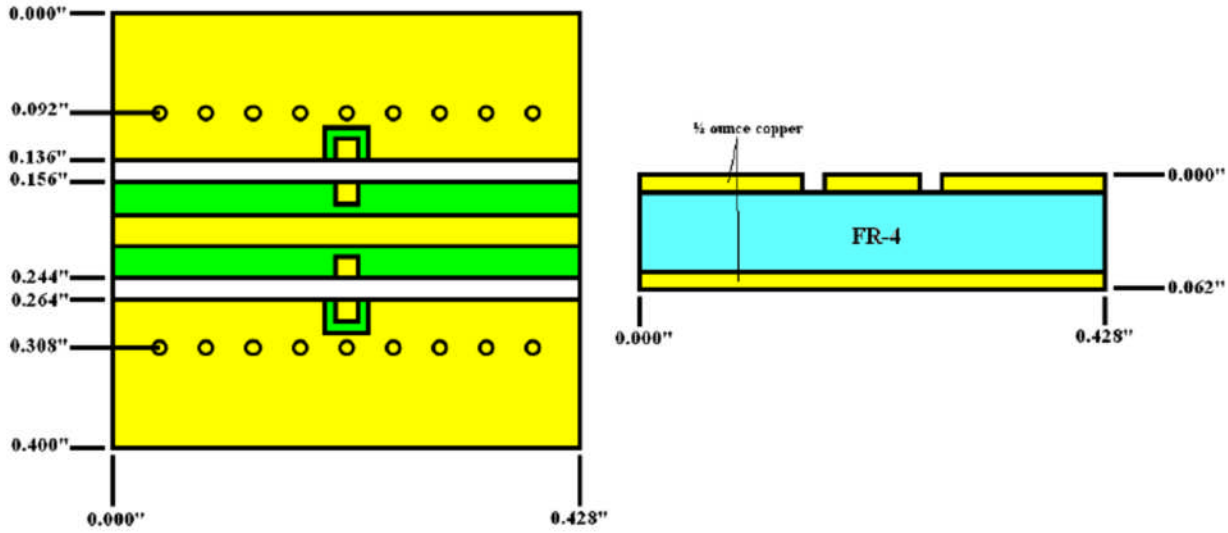


Fig. 7b) Eye Diagram 50 ohm test card

The test method consisted of a digital signal sending a series of high and low voltage pulses. In order to gauge the effect of a component on a digital signal one can sample the signal in both a high and low state and superimpose the two on each other. Distortions can be seen by repeatedly sampling the digital signal.

Results:
Testing confirms that in the off state an MLV exhibits behavior to a precision capacitor [2]. Regardless of the component type, capacitance causes distortion in digital signals (see figure 8).

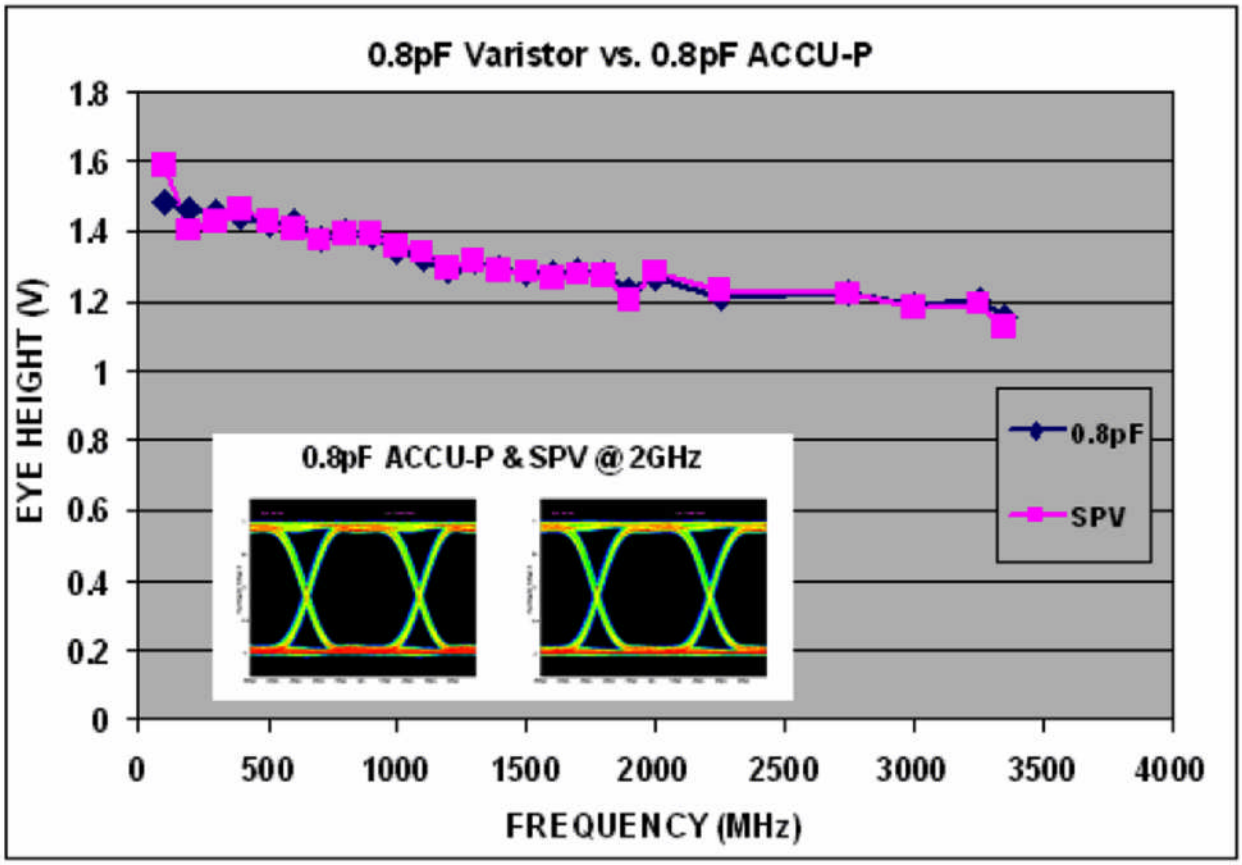


Fig.8. Eye Height vs Frequency for 0.8 pf varistors and 0.8 pf capacitor

The type of card onto which a transient suppressor is mounted greatly impacts the overall performance of the system. An unpopulated test card represents a best case scenario for constructing an eye diagram since it has no added capacitance from the transient protection device. A study was performed to determine capacitance for a variety of high speed applications. All values of eye height and eye width were normalized to an empty test board measured at the same frequency.
It was found that in order to maintain less than 10% deviation from an empty board signal for a USB-HS application a device up to ~ 8pf can be utilized in the circuit. However for ESD protection in a PCIE Gen2 system, only devices with a capacitance < 2 pf would meet the 10% performance degradation criteria used in the study. It was observed that only sub pf devices maintain an eye height that is approximately equivalent to the empty test card for the maximum frequency of our instrument 3.35GHz. See figure 9.

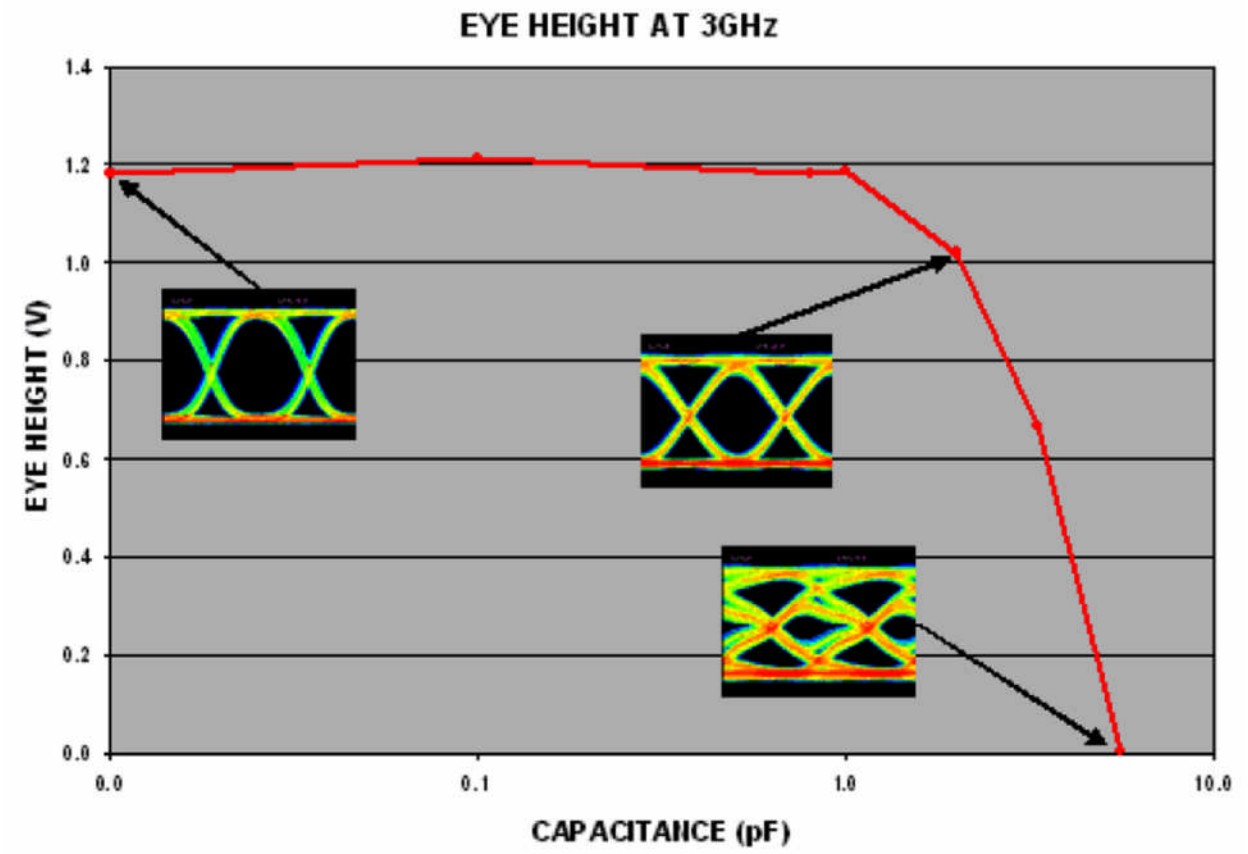


Fig.9. Effect of Capacitance on Eye Height

Summary

- Complex applications such as ESD/EMI can be used to illustrate the effect internal design and materials have upon device performance
- MLCC solutions for TVS are limited to transient integration, not clamping
- MLVs can be optimized for ESD/EMI purposes with electrode configuration modifications
- Non overlapping electrodes as well as novel material systems allow TVS device capacitances to levels as low as 0.05 pf
- Eye diagram comparisons are effective tools in determining the maximum capacitance allowed in high speed circuitry

References

[1] A Multilayer Approach to Transient Voltage Suppressors Maxwell, Chan, Templeton AVX Tech Paper

[2] Sub-pf Varistor Applications Note 1: Capacitance Effects on High Speed Circuits
Dr Eran Jones AVX APTC R&D technology report

NORTH AMERICA
Tel: +1 864-967-2150

ASIA
Tel: +65 6286-7555

CENTRAL AMERICA
Tel: +55 11-46881960

EUROPE
Tel: +44 1276-697000

JAPAN
Tel: +81 740-321250