TECHNICAL PAPER

AC Termination for Signal Busses

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Abstract
The predominant direction of modern electronic system design is towards higher speed and efficiency. This is not to say that efficiency was not an issue in previous designs, but as clock speeds increase, many elements that once were treated as ideal cannot be treated in this manner any longer. Digital system designers are faced with critical issues dealing with maintaining signal integrity while balancing numerous other inhibiting factors. Perhaps one of the more menacing non-ideal effects can be seen in signal transmission through bus lines. Gone are the days when a trace of metal could be treated as a loss less element. Today's high speed busses require a thorough evaluation using transmission line techniques. Factors such as propagation delays, signal reflections, and power consumption must be taken into account when designing high speed digital systems. Effective signal line termination maximizes the performance of the whole system by improving signal integrity while abiding by all other constraints. The termination technique dealt with in this paper is AC termination which is simply the connection of a resistor in series with a capacitor to ground.

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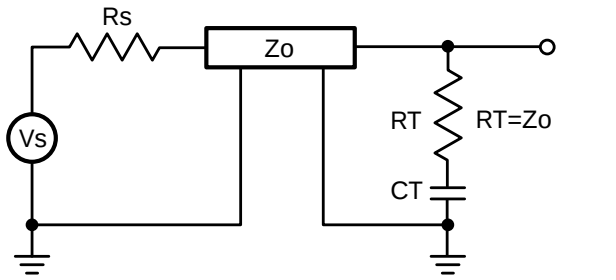
Introduction: AC Termination Basics

The principal function of a bus terminator is to maintain signal integrity while minimizing propagation delays and power consumption. Complete signal integrity is achieved by eliminating all reflections on the bus or transmission line. As can be seen by Equation 1 (Load Reflection Coefficient), the load impedance must equal the impedance of the transmission line to suppress reflections at the load. The logical choice would be to simply terminate the signal line with a resistor or resistor network equal to the characteristic impedance of the line. Unfortunately, in today's high speed low power systems this is not a viable solution because the resistor or resistor network consumes too much DC current

$$\Gamma_L = \frac{ZL - Zo}{ZL + Zo}$$

Equation 1: Load Reflection

If ZL = Zo then Reflection = 0



Vs is the source Voltage
Rs is the source Resistance
Zo is the Transmission Line Characteristic Impedance

Figure 1. AC Termination Configuration

resulting in power loss. An alternative is AC termination shown in Figure 1. Essentially, the resistor provides the impedance match needed to minimize reflections at the load. The capacitor's function is to block the DC average current thus alleviating problems dealing with power consumption. Obviously AC termination does not come without some constraints. The disadvantages are propagation delays and potential jitter errors that must be accounted for by the designer in the timing budget.

Methodology: Choosing a Capacitor

Ultimately, bus termination component values are contingent upon the actual input signal's rise time. If the rise time is greater than twice the loaded propagation delay of the bus, then termination is not necessarily needed. With relatively short lines, the signal is still rising during the signal's propagation and the reflections that are induced add to the rising edge of the signal. If the rise time is less than twice the loaded propagation delay then termination is needed. The reflections of longer lines appear as an overshoot and undershoot which degrades signal integrity.

If *tr* > *td* then termination is not necessarily needed

If *tr* < *td* then termination is needed

Choosing a capacitor for AC termination is by no means a trivial process. Tradeoffs must be analyzed for each specific system. If the RC time constant is too small then the received signal will exhibit a ringing (overshoot and undershoot) effect. If the RC time constant is too large potential jitter and power consumption become issues that the designer must confront. With this in mind, a general rule of thumb is that the RC time constant should be larger than twice the loaded propagation delay. In some instances this might not be the most desirable choice. In regards to noise margins, if some overshoot and undershoot are allowed, noise margins are increased due to the higher and lower voltage levels that the load sees. By allowing higher and lower voltages, the system state changes are more flexible thus increasing the system's immunity to noise.

Each specific design has its own unique attributes that must be evaluated from the designers perspective. In the case where there is only one device load, the calculations for the capacitor are not as extensive in that loading does not need to be considered. In this case

$$Vdiff = Ei[1 - e^{\frac{-t}{\tau}}]$$

Equation 2: Capacitor Calculatio

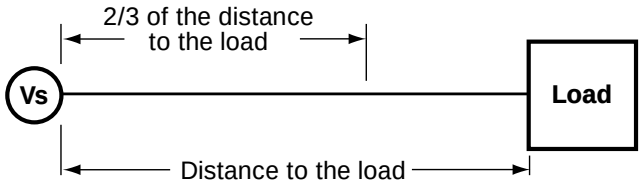
Where Ei is the incident wave related to the source b

Equation 3 $$Ei = Vs \times \frac{Zo}{Zo + Rs}$$

Where Vdiff is the difference in reference to Ei

Where $t = 2 \times time\ delay(td)$ and $\tau = 2ZoC$

Equation 2 is used to determine an effectual value for a given source impedance and allowable voltage overshoot or undershoot. Equation 3 illustrates that the performance of the terminator is significantly affected by the input source's resistance. The designer must recog-



First Load extension should be at least 2/3 distance to the load

Other Loads should be separated by .5 inch spacings

Figure 2. Two-thirds rule used in loaded network design

nize the limitations of the system and address this circumstance accordingly.

Different problems arise when the network is loaded with more than one load. When the bus is heavily loaded, at certain points on the line, reflections cause oscillations that are detrimental to logic translation. One method of minimizing reflection problems is the two-thirds rule which is shown in Figure 2. By using the two-thirds rule and spacing the loads at .5in distances from one another, reflection problems due to load clustering are avoided. Equations 4 and 5 are then used to adjust the propagation delay and characteristic imped-

Equation 3: $Zo = Zo/\sqrt{1 + \frac{CD}{CO}}$ ohms

Equation 4: $td = td \times \sqrt{1 + \frac{CD}{CO}}$ ns/inch

Where CD is the load distributed capacitance and CO is the trace intrinsic capacitance

ance. Finally, Equation 2 is used to calculate the value of the capacitor needed. There is limitation to this process, however, because the waveform's integrity is maximized only for the end load. The other loads on the network may not have acceptable time delays or voltage levels. The designer is again confronted with the aspect of accepting some overshoot at the end load by adjusting the RC time constant to provide the rest of the loads with a sufficient waveform. Timing budgets will also have to be scaled to meet specific criteria.

Recent advances in technology have allowed cofiring resistive material systems with common dielectric material systems. In conventional cofired chip carriers using LTCC materials, typical dielectric thickness ranged from 80-100µm. AVX's new revolutionary material system allows for dielectric thickness control as low as 10-15µm using very stable Class I dielectrics. Significant gains in volumetric efficiency, device resiliency, and electrical performance are apparent accolades of the new technology.

Conclusions

The objective to bus termination is simply to provide the load with an appropriate control signal while diminishing potentially adverse effects caused by signal transmission. In essence, AC termination is an extremely viable solution to bus termination. AC termination maintains signal integrity, minimizes power consumption, reduces crosstalk, and improves bus reliability. AC termination can be used to terminate both clock and data signal busses in any electronic system that utilizes CMOS and/or TTL technology. AC termination is not recommended for use in memory systems due to the varying characteristic impedances of memory lines, and high current drivers such as ECL. Also, AC termination does have a disadvantage in that a long string of successive like signal states can cause jitter errors because the capacitor charges towards the driver level and when switched, takes a longer time to charge or discharge to the appropriate level. In conclusion, each specific design comprises of numerous unique features and must be thoroughly evaluated and simulated by the designer to find the best possible solution. Nevertheless, AC termination provides substantial benefits to most applications and is a very effective method of bus termination.

Design Considerations

The following contains a few design strategies that help to alleviate some design constraints.

- Make sure that the signal driver has sufficient current and phase margin
- Use the two-thirds rule and make sure the loads are evenly distributed
- Make the minimum space between the loads .5in
- Avoid stubs and T's that cause impedance discontinuities
- Account for the loading of the loads as well as the loading for sockets and vias
- Ensure that minimum distances are required during layout
- Avoid bundled parallel signal lines whenever possible
- Ensure that there are no ground faults between circuitry connections
- Design with scaled loading effects in mind

Bibliography

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