TECHNICAL PAPER

Decoupling: Basics

Arch Martin

KYOCERA AVX Components Corporation
Myrtle Beach, S.C.

Abstract
This paper discusses the characteristics of multilayer ceramic capacitors in decoupling applications and compares their performance with other types of decoupling capacitors. A special high-frequency test circuit is described and the results obtained using various types of capacitors are shown.

Introduction

The rapid changes occurring in the semiconductor industry are requiring new performance criteria of their supporting components. One of these components is the decoupling capacitor used in almost every circuit design. As the integrated circuits have become faster and more dense, the application design considerations have created a need to redefine the capacitor parameters and its performance in high-speed environments. Faster edge rates, larger currents, denser boards and spiraling costs have all served to focus upon the need for better and more efficient decoupling techniques.

As integrated circuits have grown, so has the demand for multilayer ceramic capacitors.
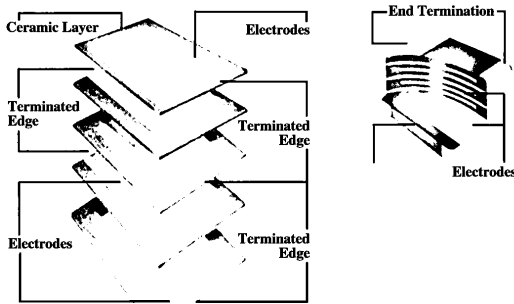
The phenomenal growth of multilayer ceramic capacitors over the last few years has been a result of their ability to satisfy these new requirements. We at AVX are continually studying these new requirements from the application view in order to better define what is required of the capacitor now and in the future, so that we can develop even better capacitor designs. Some results of these studies are the subject of this paper.

Background

A capacitor is an electrical device consisting of two metal conductors isolated by a nonconducting material capable of storing electrical charge for release at a controlled rate and at a specified time. Its usefulness is determined by its ability to store electrical energy.

An equivalent circuit for capacitors is shown in Fig. 2. This equivalent circuit of three series impedances can be represented by one lumped impedance which is used as a measure of the capacitance (Fig. 3). In other words, the amount of coulombs stored are not measured; what is measured is the lumped impedance and from this value an equivalent capacitance value is calculated.
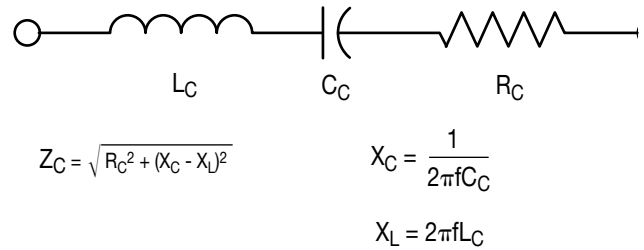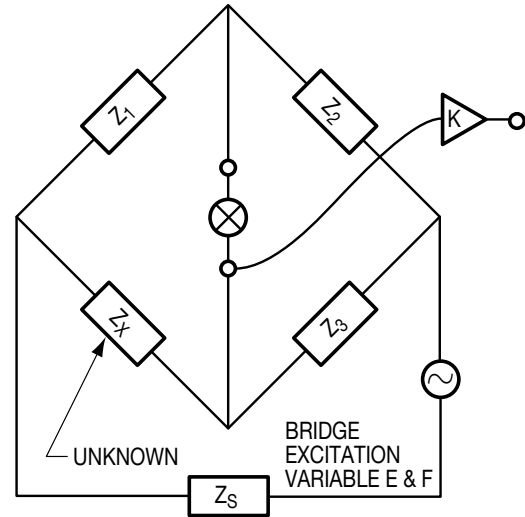

$$Z_C = \sqrt{R_C^2 + (X_C - X_L)^2} \qquad X_C = \frac{1}{2\pi f C_C}$$

$$X_L = 2\pi f L_C$$

Fig. 2. Total capacitor impedance

$$Z_X = \frac{Z_1 Z_3}{Z_2} \quad \text{(When } Z_X <\!\!<\!\!< Z_3\text{)}$$

$$Z_X = \frac{|Z_1| \cdot |Z_3|}{Z_2}$$

$$\theta_X = \theta_1 + \theta_3 - \theta_2$$

Fig. 3. Basic impedance bridge

Thus capacitance as measured is actually a combination of the capacitive reactance, the inductive reactance and the equivalent series resistance.

As shown in Fig. 4, all three of these series impedances vary differently with frequency. Since all three vary at different rates with frequency, the capacitance calculated from the resultant impedance is made up of different components at different frequencies. This can be seen by increasing the lead length of a capacitor while it is being measured at 1 MHz on an equivalent series capacitance bridge and watching the capacitance increase. Increased inductance (increased lead length) actually increases the capacitance value read by the capacitance bridge (Fig. 5).
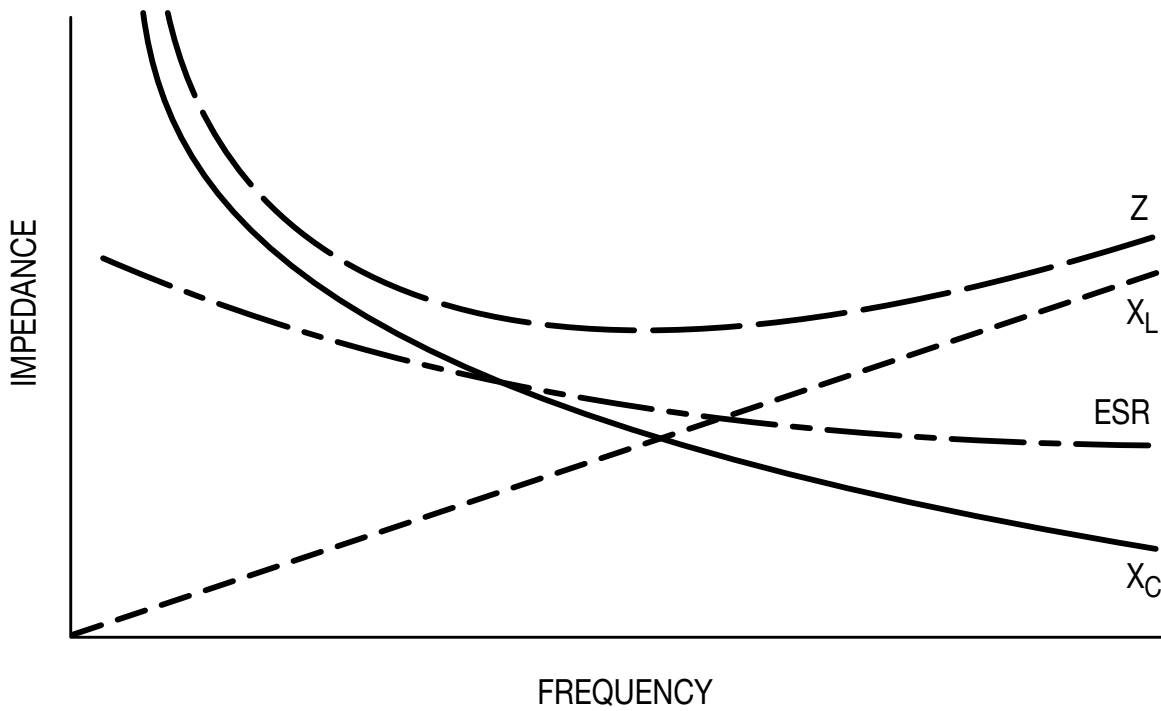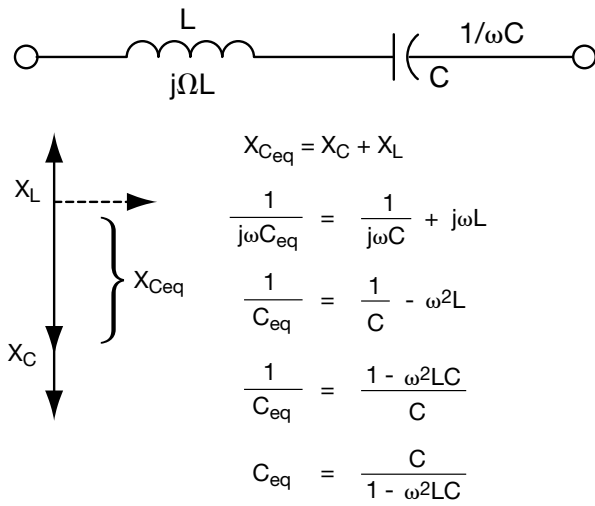
Fig. 4. Variation of impedance with frequency

$$X_{C_{eq}} = X_C + X_L$$

$$\frac{1}{j\omega C_{eq}} = \frac{1}{j\omega C} + j\omega L$$

$$\frac{1}{C_{eq}} = \frac{1}{C} - \omega^2 L$$

$$\frac{1}{C_{eq}} = \frac{1 - \omega^2 LC}{C}$$

$$C_{eq} = \frac{C}{1 - \omega^2 LC}$$

AS "L" INCREASES "C_{eq}" INCREASES
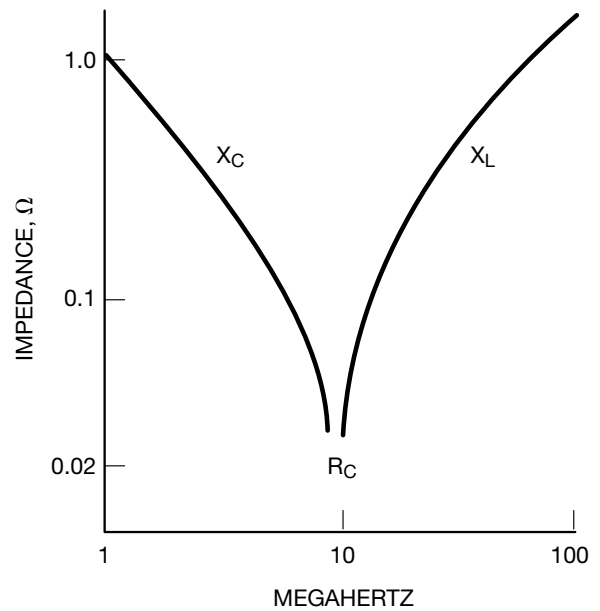
Fig. 5. Effects of inductance

Fig. 6. Major impedance components

The major components of a typical impedance curve vs. frequency are shown in Fig. 6. Below resonance, the major component is capacitive reactance, at resonance it is equivalent series resistance, and above resonance it is inductive reactance. In decoupling today's high-speed digital circuits the capacitor is primarily being used to eliminate high-speed transient noise which is above its resonance point, an area where inductive reactance is the major impedance component. In these applications it is desirable to maintain as low an inductance or totol impedance as possible. For effective and economical designs it is important to define the performance of the capacitor under the circuit conditions in which it will be used.

High-Frequency Testing

The test schematic shown in Fig. 7 can be used to determine the performance of various styles of capacitors at high frequencies. Lead lengths are minimized through the use of the test fixture shown in Fig. 8. This test set-up is intended to duplicate the performance of the capacitor under actual use conditions. The Hewlett-Packard current generator supplies high-frequency pulses equivalent to an actual digital IC circuit. Edge rates of 200 mA/10 ns or 200 mA/5 ns are fed to the capacitor to determine its performance. Edge rates in the 5 to 10-ns range were chosen for testing since transients in this range are common to many designs such as shown in Fig. 9, where transients in the 5 to 10-ns range occur regularly on a DEC VAX 11/780 memory board using Mostek 4116 dynamic RAMs.
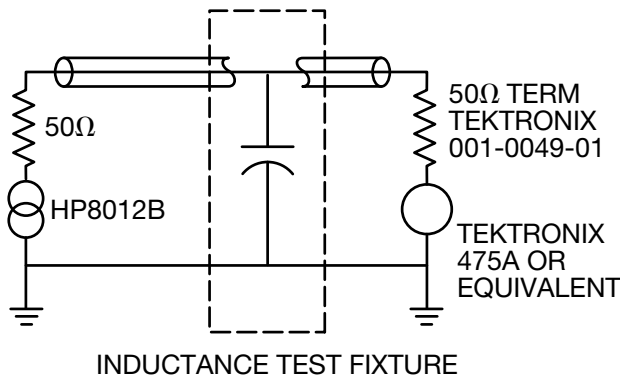
INDUCTANCE TEST FIXTURE
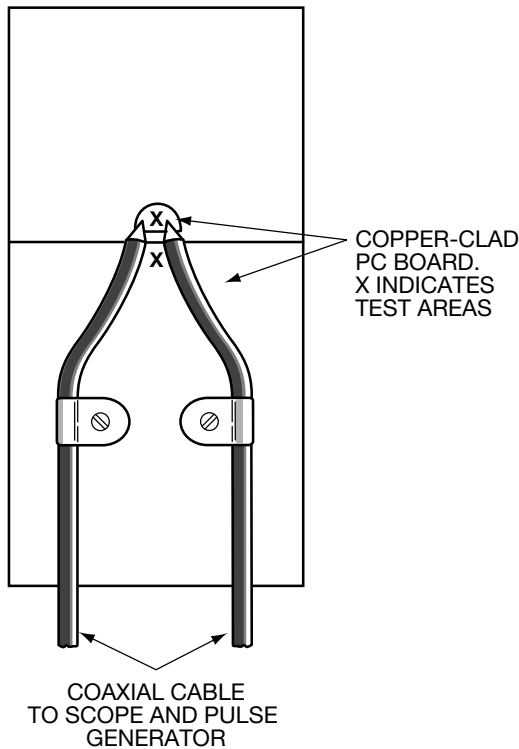
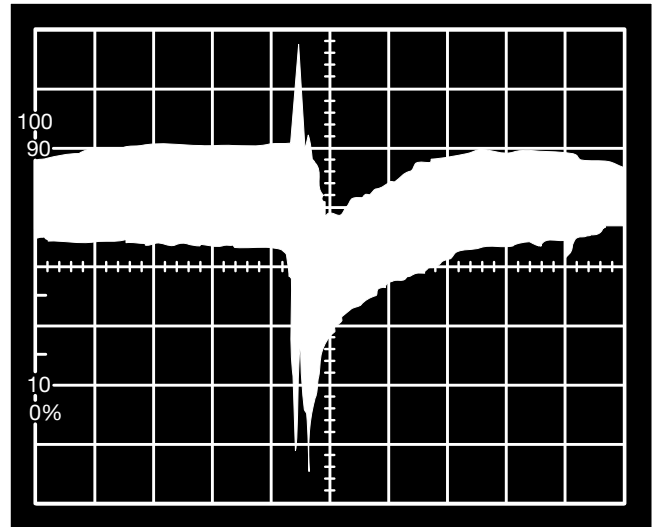**Fig. 7.** High-frequency test schematic

Fig. 8. Inductance test fixture
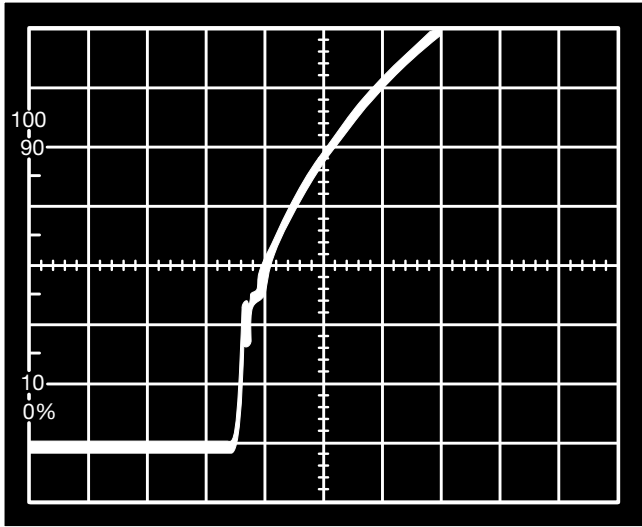
SCALE:
HORIZONTAL = $1\mu S$/DIV
VERTICAL = 5MV/DIV

Fig. 9. Transients from V_{DD} to V_{SS} in 256K byte dynamic memory (Mostek 4116) in DEC VAX 11/780

All three components (capacitive, resistive, and inductive) are evident on the scope trace (Fig. 10) obtained by using the test circuit of Fig. 7. Thus the performance of a capacitor can be described under typical use conditions for capacitance ($C = I \frac{dt}{dv}$), equivalent series resistance ($ESR = V_A/I$), and inductance ($L = V_L \frac{dt}{di}$). This information can then be used to select a capacitor having the required characteristics for the application.
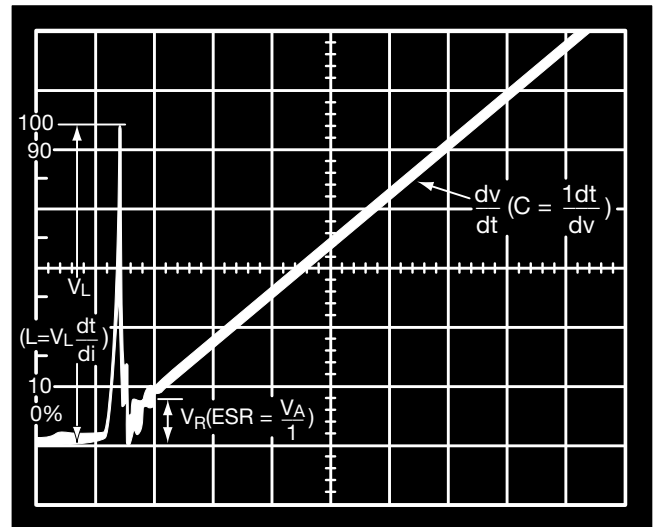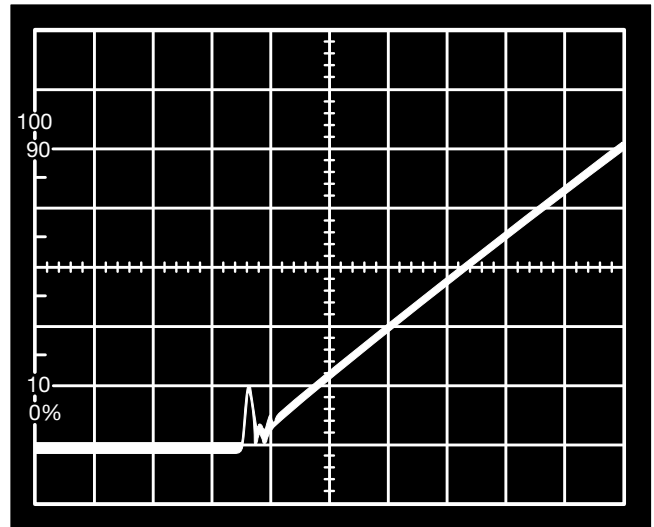
SCALE:
HORIZONTAL = 50NS/DIV
VERTICAL = 50MV/DIV

Fig. 10. Scope trace of 0.22-µF film capacitor using test setup of Fig. 7 and 200 mA/10 ns input

SCALE:
HORIZONTAL = 50NS/DIV
VERTICAL   = 100MV/DIV

Fig. 11 (A). Scope trace of 0.1-µF tantalum capacitor using test setup of Fig. 7 and 200 mA/10 ns input

SCALE:
HORIZONTAL = 50NS/DIV
VERTICAL   = 100MV/DIV

Fig. 11 (B). Scope trace of 0.1-µF multilayer ceramic capacitor using same test setup and input

Test Results

Figures 11(A) and 11(B) compare the results of testing a 0.1-µF rated multilayer ceramic capacitor with a 0.1-µF rated tantalum capacitor. The slope of the curve, dv/dt, is a measure of the capacitance in the time domain of interest. For the ceramic this is approximately 0.1 µF but for the tantalum the value is 0.05 µF or approximately half the capacitance of the ceramic.

Another way to state this is at constant current:

$$C_{Tantalum} \frac{dv}{dt} = I = C_{Ceramic} \frac{dv}{dt}$$

$$C_T \frac{0.2}{50 \times 10^{-9}} = C_C \frac{0.1}{50 \times 10^{-9}}$$

$$C_T = \tfrac{1}{2} C_C$$

The induced voltage generated in response to the 200 mA/10 ns edge rate can be used to determine the inductance of the capacitor. Under these conditions the tantalum shows 2.5 times the inductance of the multilayer ceramic (MLC) capacitor:

$$L = V_L \frac{dt}{di}$$

Ceramic **Tantalum**

$$L = 0.1 \frac{10 \times 10^{-9}}{0.2} \qquad L = 0.25 \frac{10 \times 10^{-9}}{0.2}$$

$$L = 5.0 \text{ nH} \qquad L = 12.5 \text{ nH}$$

The ESR is obtained from the minimum voltage reached after the voltage spike. In the case of the ceramic the ESR is too small to measure on the scale used, i.e., less than 5 mΩ. The ESR for the tantalum can be determined with the V_R = 150-mV reading giving an ESR = 750 mΩ.

Both the MLC and the tantalum capacitors were tested with equal lead lengths. Removal of the leads reduces the inductance obtained for the MLC (now an MLC chip capacitor) to V_L = 20 mV for an inductance of 1 nH.

This test procedure can be used to compare the performance of various styles of capacitors. Fig. 12 compares the performance of MLC and a film capacitor. Both units show dv/dt equivalent to the capacitance values read at 1 kHz (0.22 µF for the film and 0.20 µF for the MLC). The MLC shows a voltage spike of 75 mV vs. the 275-mV spike for the film, i.e., the film had 3.7 times the inductance of the MLC. In addition, the MLC had half the ESR of the film capacitor.

The initial voltage spikes found from an input of 200 mA/5 ns edge rate are given in Table I for various capacitor values and styles. The equivalent inductances for these values are shown in Table II. These results are based on essentially zero lead lengths for all types. From a practical standpoint, the lead length inductances shown in Table III must be added to values of Table II in order to mate the capacitor with the PC board.

```
100
90

        0.22µF FILM

        0.20µF CERAMIC

10
0%
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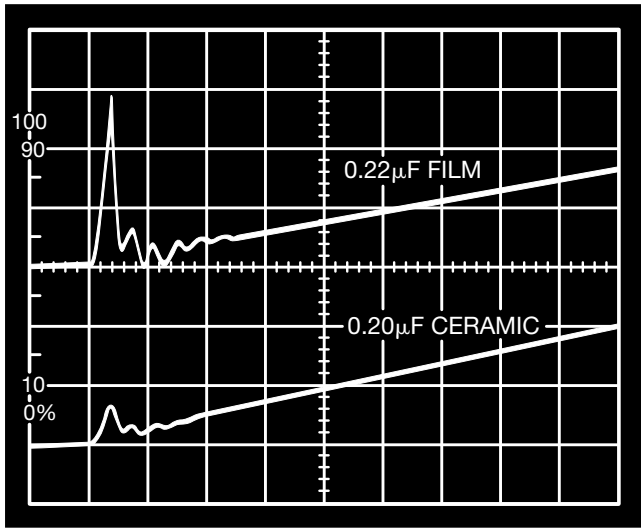
SCALE:
HORIZONTAL = 20NS/DIV
VERTICAL = 100MV/DIV

Fig. 12. Comparison of 0.2-µF MLC with
0.22-µF film capacitor

CAPACITOR	.01µF	.1µF	.22µF	1.0µF	2.2µF
FILMS:					
BRAND A	170	240	—	470	—
BRAND B	110	120	120	140	—
BRAND C	180	300	—	350	—
BRAND D	300	—	230	—	—
TANTALUMS:					
BRAND E	—	380	—	380	—
ALUMINUMS:					
BRAND F	—	630	—	400	—
AVX MLC'S					
CONFORMAL					
RADIALS	—	70	—	70	90
MOLDED					
RADIALS	—	—	—	50	—
DIP'S	—	50	40	—	—
MOLDED					
AXIALS	80	130	140	210	—

Table I. Voltage spikes (mV) from 200 mA/5 ns edge rate
with essentially zero lead lengths

CAPACITOR	.01µF	.1µF	.22µF	1.0µF	2.2µF
FILMS:					
BRAND A	4.3	6.0	—	11.8	—
BRAND B	2.8	3.0	3.0	3.5	—
BRAND C	4.5	7.5	—	8.8	—
BRAND D	7.5	—	5.8	—	—
TANTALUMS:					
BRAND E	—	9.5	—	9.5	—
ALUMINUMS:					
BRAND F	—	15.8	—	10.0	—
AVX MLC'S					
CONFORMAL					
RADIALS	—	1.8	—	1.8	2.3
MOLDED					
RADIALS	—	—	—	1.3	—
DIP'S	—	1.3	1.0	—	—
MOLDED					
AXIALS	2.0	3.3	3.5	5.3	—

Table II. Inductances (nH) from 200 mA/5 ns edge rate
with essentially zero lead lengths

CAPACITOR TYPE	TYPICAL LEAD LENGTH (MM)	LEAD L (NH)	LEAD V_L (MV)	LEAD IMP. (Ω)
FILMS:				
BRAND A	3.81	1.5	60	0.9
BRAND B	2.54	1.0	40	0.6
BRAND C	3.81	1.5	60	0.9
BRAND D	2.54	1.0	40	0.6
TANTALUMS:				
BRAND E	5.08	2.0	80	1.3
ALUMINUMS:				
BRAND F	4.45	1.8	70	1.1
AVX MLC'S				
CONFORMAL				
RADIALS	2.54	1.0	40	0.6
MOLDED				
RADIALS	2.54	1.0	40	0.6
DIP'S	5.08	2.0	80	1.3
MOLDED				
AXIALS	7.62	3.0	120	1.9

Table III. Typical lead lengths required to connect capacitor to
PC board

Decoupling

The above capacitor models can be used to optimize the decoupling of integrated-circuit designs. As an example, the decoupling requirements of dynamic RAMs will be discussed. Dynamic RAMs have large transients which are generated during their refresh cycle. These large transients require careful attention to the decoupling techniques to avoid "V bump" or "soft" error problems.
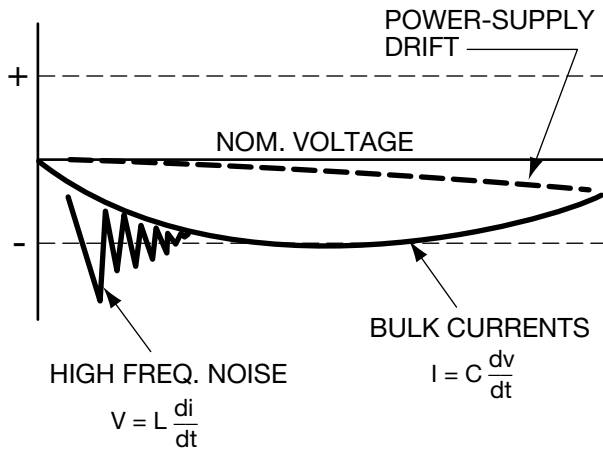

Fig. 13. Three factors causing voltage variations

The function of the capacitor can be illustrated by referring to Fig. 13. Through time, the three factors causing voltage variations are: dc drift, bulk variations, and switching transients. Dc drift is independent upon power-supply design and not on the board level decoupling. Bulk variations come about by the current demands of recharging the internal storage cells during the refresh cycle. Transient "noise" comes from switching currents internal to the IC chip. The total of these three voltage variations must be maintained within the allowed tolerance for the IC device. In other words, if the voltage drops below the operating margin of the IC, a "soft" error will occur.

The board low-frequency surge current to be supported by the bulk capacitance is effectively the IC's average refresh active current for the length of a refresh cycle. This can be determined by referring to the IC spec (and assuming worst-case that stand-by current is zero and active current is maximum). The traditional approach for calculating bulk capacitance requirements is to multiply the capacitance needed per package times the number of packages on the board. This arrives at the total capacitance required, which is then approximated with large-value capacitors around the periphery of the circuits.

It is more effective to distribute this capacitance throughout the design with smaller value capacitors whose combined total meets or exceeds the bulk-current requirement. Distribution of the bulk requirement to capacitors adjacent to the current requirements (the IC chip) is beneficial in reducing

inductance and resistive voltage drops. Slight increases in the distributed transient capacitor values can typically eliminate the need for large capacitors to supply bulk current.

Transient noise is commonly called in the industry "V bump," and reflects the supply transient induced by the chip itself on the decoupling capacitor when various clocks fire on-chip and drive on-chip capacitance associated with that event (such as address decoding). Since actual loads switched are small (20 pF), the size of the decoupling capacitor is less important than its inductance.

Using capacitors for reducing the line "noise" that comes from switching internal to the IC chip requires low inherent inductance within the decoupling capacitor and effective board design. Multilayer ceramic capacitors are available in values high enough to meet distributed bulk requirements while maintaining low inductance at high frequencies.

When a capacitor is mounted on a board, lead lengths and board lines (device to capacitor to ground) are a major source of inductance. This inductance must be minimized to obtain good decoupling performance under high-speed transient conditions. Minimum lead lengths, wiring, and gridding of power supplies and ground with alternate parallel paths are important as is the quality of the capacitor (Fig. 14). The use of multiple capacitors instead of a few large bulk capacitors can be used to decrease line lengths and to increase path numbers (gridding) for reduced inductance and more effective surge-current availability.
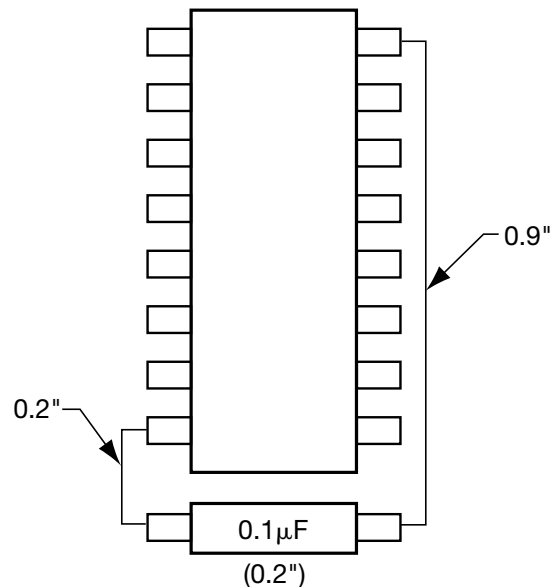

Fig. 14. Circuit board line and capacitor lead lengths

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