TECHNICAL PAPER

The Effects of ESR and ESL in Digital Decoupling Applications

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Abstract

It is common place for digital integrated circuits to operate at switching frequencies of 100 MHz and above, even at the circuit board level. As these frequencies continue to increase, the parasitic of the decoupling capacitors must be considered. A study on the effects of equivalent series resistance (ESR) and equivalent series inductance (ESL) in a typical digital decoupling application is presented. Utilizing SPICE, it can be shown that the ESR and ESL of chip capacitors can dramatically alter the voltage seen by the integrated circuit (IC). By changing the values of the parasitics and comparing the results to the ideal case for a variety of frequencies, some common decoupling design rules are formulated.

KYOCERA AVX

THE EFFECTS OF ESR AND ESL IN DIGITAL DECOUPLING APPLICATIONS

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Introduction

The use of monolithic capacitors to decouple digital circuitry is certainly nothing new [1,2]. But as microprocessor clock speeds increase, what appears to be daily, the need to better understand the parasitic effects of capacitors in the decoupling of integrated circuits (ICs) becomes more important. Instead of studying one particular type, such as a ceramic chip, tantalum chip or any other type of surface mount capacitor, this work focuses on the general behavior of these devices. By doing this, the designer can make informed decisions on which capacitor value and type to use for a given application. This work does not cover the effects on capacitance such as voltage and temperature dependencies, as it is assumed that the designer knows the capacitance for the given environmental and bias conditions.

The simplest equivalent circuit for a capacitor can be most generally realized as

with the magnitude of the impedance given as

$$|Z_C| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C_C}\right)^2} \qquad [1]$$

where ω is 2πf. There are much more complicated models that can be created, especially with tantalum capacitors, but for most general purposes the above model does the job.

As many ways there are to mount a decoupling capacitor near an IC, is a many ways to model the interconnect between the power supply and the IC. The number of "ways" is probably infinite and so for this work a typical case for a multi-layered printed circuit board (PCB) is used. Due to the small impedance from the power supply to the decoupling capacitor (due to the power/ground planes imbedded in the PCB), the inductance of a typical via/pad connection is around 400 pH. The value for the inductance from the capacitor to the IC can vary dramatically, depending on the line width, layer thickness, dielectric constant of the PCB, etc. For this work, a value of 1 nH was chosen for the inductance of the interconnect between the cap and the IC. Once again this value can vary widely and to cover all the variations of this value is beyond the scope of this work.

Perhaps the most difficult device to model is the IC chip. As in most CMOS circuitry, the chip only draws current when the transistors are switching and only a leakage current during the "0" or "1" state. No two different ICs have the same amount of transistors, so the amount of current drawn, the number of gate capacitors to be charged and the rate at which the gate capacitors are charged varies greatly. Some IC vendors actually publish models of the µprocessor as in [3]. To keep the results of this work as general as possible, the IC will be modeled as a simple current sink. The slew rate and the maximum current can easily be varied by choosing such a device. The waveform for a 100 MHz, 0.5A/ns waveform is shown in Figure 2.

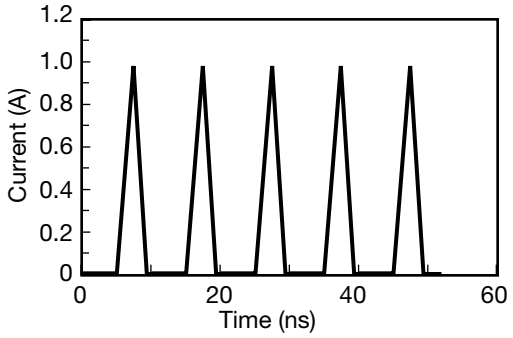

Figure 2. Typical IC current waveform.

Finally, the complete modeling circuit used for this work is shown in Figure 3. This is a very simplified circuit from the actual case, but it helps to understand the effects of the capacitors located closest to the IC. One needs to keep in mind that the circuit in Figure 3 concerns itself with only one power/ground pin of the IC. Today's high performance ICs contain as many as 300 pairs of power/ground pin sets.

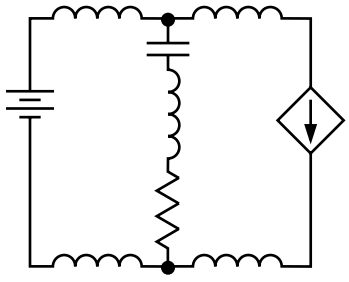

Figure 3. Decoupling circuit model.

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Choosing A Decoupling Capacitor The Ideal Case

One method proposed [2] to choose a decoupling capacitor lies in the fact that we know:

$$Q = CV \tag{2}$$

and

$$\frac{dQ}{dt} = I = C\frac{\Delta V}{\Delta t} \tag{3}$$

$$C = I\frac{\Delta t}{\Delta V} \tag{4}$$

That is to say, for a desired maximum ripple voltage, ΔV, a switching time of Δt and a peak current of I, the minimum decoupling capacitor needed is C.

There are a couple of interesting observations from [4]. The first being that the needed capacitance is indirectly proportional to the ripple voltage. This comes as no big surprise. However, [4] also states that the faster one can switch the current in the IC, the less decoupling capacitance is needed. In an ideal world this may be true, but the addition of parasitic inductance and resistance can easily override this aspect of equation [4], as will be demonstrated later.

If the ideal case of [4] is used in the circuit of Figure 3, with no parasitic inductance or resistance, the resulting waveform is very close to ideal. As example we will use a 0.01, 0.1 and 1µF capacitor to decouple a 0.5A/ns current sink with a peak current of 1A. Using [3], the resulting voltage should be around 50mV for the 0.01µF case and the Spice results shown in Figure 4.

As is plainly shown in Figure 4, the ideal equation [4] for the voltage is already breaking down, because of the introduction of the trace inductances between the capacitor and the IC.

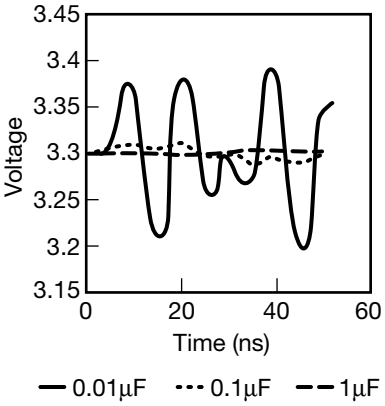

Figure 4. Ripple voltage on ideal decoupling capacitor using a 0.01, 0.1 and 1µF.

Effects of ESR on Decoupling

Using the circuit in Figure 3, let's examine the effects of ESR on the arc voltage swing over the capacitor. Keep in mind that this work concentrates on the overall view of ESR in general, as opposed to specific devices. The current sink used here is the same as in Figure 2 and the capacitor value is 0.1µF.

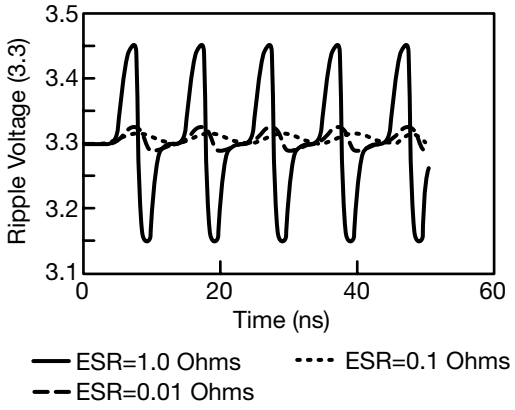

Figure 5. Effects of ESR on ripple voltage of 0.1µF capacitor.

As Figure 5 clearly shows, the greater the ESR of a device, an increase in the ripple voltage for a given cap value is seen. This is directly related to the RC time constant of the capacitor and is something that has been known by switch-mode power supply designers for a long time. Decreasing the resistance, decreases the ripple.

Another test of interest involves the slew rate and frequency of the IC current sink on the decoupling voltage. Figure 6 shows the resulting voltage ripple using a 0.1µF capacitor, with an ESR of 1Ω and a maximum current of 1 A. The 1W is chosen to accentuate the effects on the ripple voltage. The current sink is set for 25, 50 and 100 MHz, with rise times of 0.5, 0.25 and 0.125 A/ns, respectively. While the indirect relationship of [4] holds, the effect of the ESR on the circuit keeps the ripple voltage from being the ideal case. Once again the RC time constant comes into play, with the lower frequency clock speeds producing less ripple.

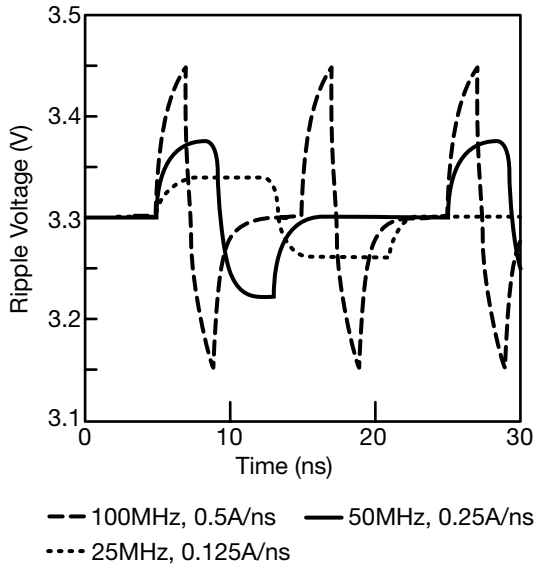

Figure 6. Slew rate and frequency effects of the current sink. Capacitance = 0.1µF, ESR = 1Ω

As a final example of the result ESR on ripple voltage, Figure 7 shows the response when the ESR is kept constant at 0.1Ω and the cap is changed. The difference in the response between the 0.1 and 1.0µF capacitors is minimal and any increase in capacitance value does not lower the ripple voltage seen at the IC. This is in direct contrast to the ideal response given in [4] and shown in Figure 7. One should not make the mistake extra cap is harmful, as the added charge helps for lower frequency noise. The addition of the resistance to the capacitor allows the device to deliver only as much charge as the controlled by the RC time constant of the capacitor.

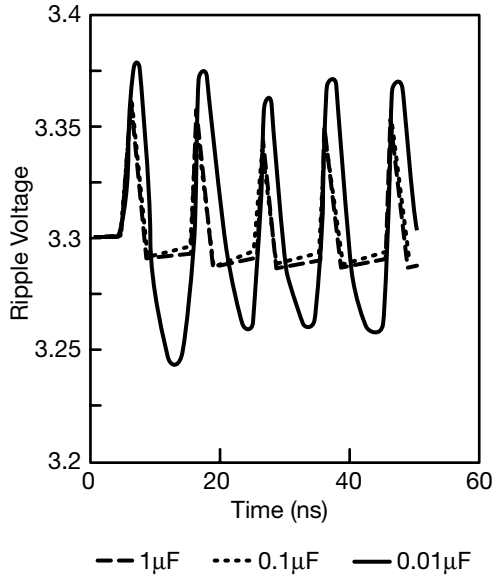

Figure 7. Effect of constant ESR on IC ripple voltag for 0.01, 0.1 and 1µF.

Effects of ESL on Decoupling

Another important parameter of the decoupling capacitor is the parasitic inductance. As the industry switched from leaded to surface mount devices, the idea of lower inductance as an aide in decoupling first became noticed. Now, there are specific, surface mount capacitors whose device physics lend themselves to a lower equivalent series inductance. Once again, to keep this paper away from specific devices and concentrating on general capacitor construction rules, only changes in parasitic inductance will be examined.

The first and most obvious case to be examined is for a given capacitance, ESR and IC current waveform, how does the ripple voltage seen by the IC change. Using the circuit described in Figure 3, with a capacitor of 0.1µF, an ESR of 0.1Ω and a slew rate of 2A/ns on the IC current, the results using different parasitic inductances are shown in Figure 8. As is plainly shown, given constant cap and ESR values, an increase in inductance will give an increase in the ripple voltage.

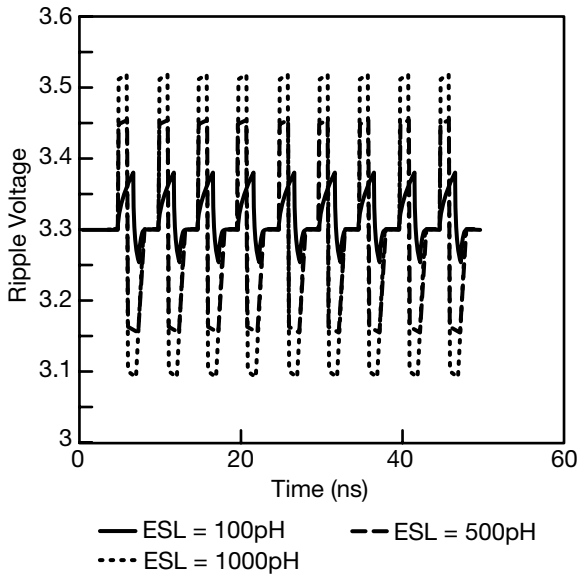

Figure 8. Effects of ESL on ripple voltage.

The above results should come as no great surprise, but what about the effect of slew rate. Using the same cap and ESR values and choosing a parasitic inductance of 500 pH, Figure 9 shows the effect of three different slew rates; .05, 1 and 2 A/ns. Using the simple formula

$$V = L\frac{di}{dt} \qquad [6]$$

one cannot solve for the peak voltage across the capacitor. The capacitive part of the device makes equation [6] useless. This is why measurement techniques to solve for the inductance of a capacitor by switching a voltage across the cap should be examined carefully.

Conclusions

This paper demonstrates the use of SPICE to simulate the decoupling of an integrated circuit device, using the full electrical model for a capacitor. For a given capacitance value, the increase of the ESR in that device will cause an increase in the ripple voltage seen by the IC. The ripple voltage cannot be decreased by increasing capacitance (the ideal case),

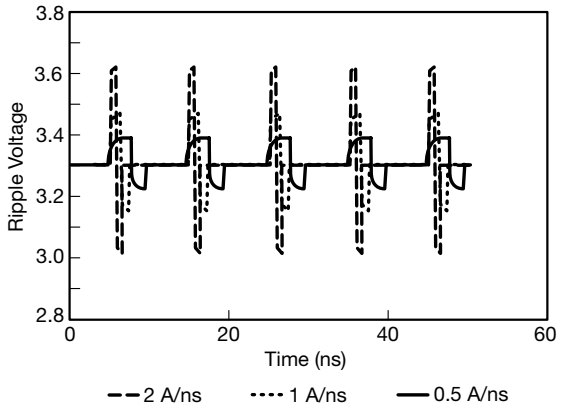

Figure 9. Slew rate effects on ESL.

once the equivalent series resistance is added. A good rule of thumb is to keep the reciprocal of the time greater than the operating frequency, or:

$$1/\tau = 1/ESR*C \sim> f. \qquad [7]$$

One needs to look very closely at the parasitic inductance of the localized decoupling caps, as this can effect the voltage ripple even more than the resistance. This is especially true on the rising and falling edges of the IC, as one would expect. Using equation [6] is a good start, but this is for only one power/ground pin set, and the effects of connecting multiple capacitors in parallel should be considered.

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