TECHNICAL PAPER

LICA® Design Guide

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Abstract

A review of high frequency decoupling basics highlighting the advantages of using LICA® with its C4 terminations in these applications.

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Introduction

The rapid changes occurring in the semiconductor industry are requiring new performance criteria of their supporting components. One of these components is the decoupling capacitor used in almost every circuit design. As the integrated circuits have become faster and denser, the application design considerations have created a need to redefine the capacitor parameters and its performance in high-speed environments. Faster edge rates; larger currents, denser boards and spiraling costs have all served to focus upon the need for better and more efficient decoupling techniques.

Background

A capacitor is an electrical device consisting of two metal conductors isolated by a nonconducting material capable of storing electrical charge for release at a controlled rate and at a specified time. Its usefulness is determined by its ability to store electrical energy.

An equivalent circuit for capacitors is shown in Figure 1. This equivalent circuit of three series impedances can be represented by one lumped impedance, which is used as a measure of capacitance. In other words, the amount of coulombs stored is not measured; what is measured is the lumped impedance and from this value an equivalent capacitance value is calculated.

Figure 1. Equivalent Series Model for a Ceramic Capacitor

Thus capacitance as measured is actually a combination of the capacitive reactance, the inductive reactance and the equivalent series resistance.

As shown in Figure 2, all three of these series impedance vary differently with frequency. Since all three vary at different rates with frequency the capacitance calculated from the resultant impedance is made up of different components at different frequencies. This can be seen by increasing the lead length of a capacitor while it is being measured at 1 MHz on an equivalent series capacitance bridge and watching the capacitance increase. Increased inductance actually increases the capacitance value read by the capacitance bridge.

The major components of a typical impedance curve vs. frequency are shown in Figure 3. Below resonance, the major component is capacitive reactance, at resonance it is equivalent series resistance and above resonance it is inductive reactance. In decoupling today's high-speed digital circuits the capacitor is primarily being used to eliminate high-speed transient noise, which is above its resonance point, an area where inductive reactance is the major impedance component. In these applications it is desirable to maintain as low inductance or total impedance as possible. For effective and economical designs it is important to define the performance of the capacitor under the circuit condition in which it will be used.

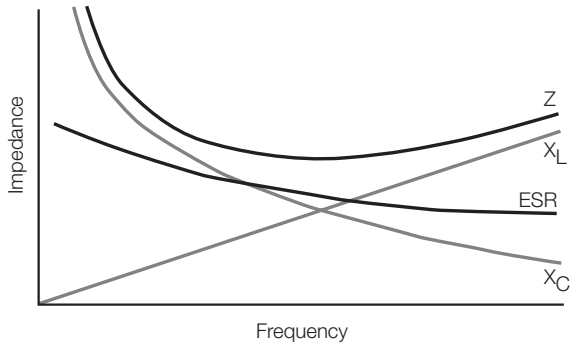

Figure 2

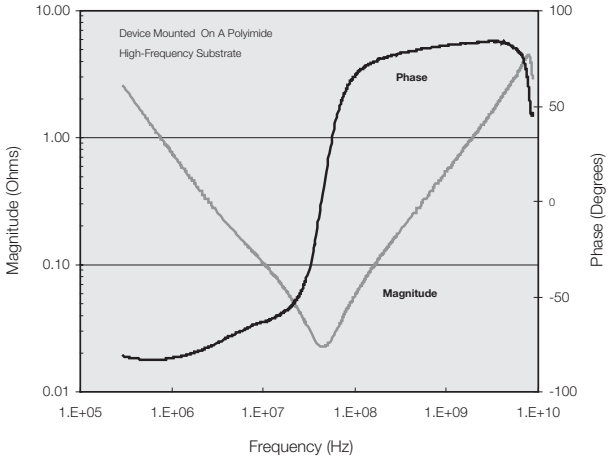

Figure 3. Typical Impedance and Phase curves for LICA® 200nF Capacitor

Decoupling

Decoupling is a means of overcoming the physical and time constraints found in a Power Distributions System (PDS) of a digital circuit. Simply put, decoupling reduces switching noise in the PDS. In a digital environment, the switching integrated circuits, power supplies and regulators mainly generate this noise, which can be thought of as voltage ripple in the PDS.

Using decoupling capacitors is one of the most common, efficient and relatively inexpensive ways to achieve better signal integrity by reducing voltage ripple. The decoupling capacitor acts as a reservoir of energy located near the point of requirement.

As shown earlier in Figure 1, a capacitor can be modeled as a simple series RLC circuit. Mathematically, the impedance of this model is given as

$$|Z| := \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2} \qquad [2]$$

where $\omega = 2\pi f$.

The Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) are the parasitics of a real capacitor. This impedance, when plotted with frequency gives the graph the "V" shape shown earlier in Figure 3.

The left side of the "V" is the Capacitive Reactance portion of the impedance curve and is given as

$$X_C := \frac{1}{\omega C} \qquad [3]$$

The right side of the "V" is the Inductive Reactance portion of the impedance curve and is given as

$$X_1 := \omega \cdot ESL \qquad [4]$$

The frequency where these two reactances are equal and cancel each other (at the bottom of the "V") is the Resonant Frequency of the capacitor and is given as

$$f_{res} := 2\pi\left(\frac{1}{\sqrt{ESL \cdot C}}\right) \qquad [5]$$

In the early days of electronics, the inductive portion of the impedance, that due to the parasitic inductance of the capacitors, did not play a major role in decoupling applications. As speeds have increased, the operating frequencies are now well into the inductive portion of the frequency range. One can visualize this inductive behavior of the capacitor as a physical constraint that reduces the capacitor's capability to deliver the quick burst of energy to the switching IC.

Now, let's quantitatively examine the effects of ESL on digital PDS. The voltage and inductance is related by the following equations:

$$V = L \cdot di/dt \qquad [6]$$

$$V = ESL \cdot di/dt \qquad [7]$$

$$V = \omega \cdot ESL \cdot I \qquad [8]$$

Equation [6] shows that a change in the current, I, will cause a voltage drop, V, in the circuit. In a digital circuit, current is drawn whenever a transistor is switched, resulting in a concurrent voltage drop. This voltage drop will ripple through the circuit resulting in possible errors. To reduce the possibility for errors at high frequencies it is critical to use decoupling capacitors with the *lowest* ESL possible. This is clear from equation [8], which shows a *reduction* in ESL results in a *reduction* in V or ripple.

Up to this point, the effect of ESL on the PDS has been shown, but what about ESR? In order to effectively decouple a PDS, it is necessary to use capacitors with the lowest ESR possible. For example, examine the effects of ESR at *lower frequency* regime. To explain this real parasitic ESR term, add Ohm's law to the voltage drop across an ideal capacitor. The equation with the parasitic ESR is shown [9].

$$V := \frac{I}{\omega C} + I \cdot ESR \qquad [9]$$

This equation shows the ESR term does not allow the voltage drop, V, to go away even if one increases the capacitance to infinity. In the real world one must *increase capacitance* and *decrease ESR* in order to decrease the ripple noise across a *broad* spectrum in the PDS.

High Frequency Decoupling

It should also be noted Equation [9] states, at higher frequencies; higher capacitance does little to reduce the voltage drop. Instead at higher frequencies decoupling is more effective with reduced inductance than with higher capacitance. The maximum amount of inductance allowed to minimize the ripple voltage is given by

$$L := V \cdot \frac{dt}{dI} \qquad [10]$$

Where dt is the fastest rise time of a transient current. For example suppose there is a 20 amp current transient with a rise time of 1nSec, and the PDS must remain within 5% of a 1.8V power supply. The amount of inductance allowed is estimated to be:

$$L = 1.8V*0.05*(1nSec/20A)=4.5pH \qquad [11]$$

Given this is a mounted inductance (hence the ESL of the capacitor must be below 4.5pH); it is difficult to find an acceptable surface mount capacitor. The designer would achieve this inductance and the target impedance by first choosing a capacitor with the lowest inductance. (The capacitance of the chosen component should not play a major role in decoupling at the higher frequencies, but one should seek the highest possible value for a given low ESL since it will lower the impedance over a broader frequency range.) A sufficient quantity of the low inductance capacitors should be placed in parallel. This requires more real estate on the board, something that is generally limited on today's designs. Thus, it is critical to use capacitors with very low inductance to reduce quantity, board space and cost.

Mounted Inductance

So far we have only investigated the inductance of the component itself. In real world applications this is only a portion of the overall inductance impacting the PDS performance. The inductance associated with traces connecting a decoupling capacitor to the power rails is often significantly higher than the parasitic inductance of the capacitor itself. As a general rule, 10nH/in trace inductance can be used to measure this inductance.

For today's high frequency decoupling applications it is crucial to minimize the loop inductance. One method (besides using low inductance capacitors) is the use of via-in-pad technology and locating them as close to the capacitor as possible. Figure (4) illustrates this.

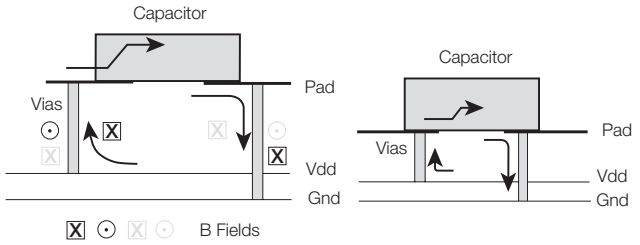

Figure 4. Inductance Developed in Current Loops

With optimum pad design, the dominate factor in mounted inductance is the height of the via and connection to the capacitor. Given this, the most obvious method for keeping inductance low is locating the ground and power plane as close to the capacitor mounting surface as possible and keeping the associated traces to a minimum.

Low Inductance Chip Arrays (LICA®)

AVX was able to design a capacitor to meet the high frequency decoupling requirements of today's high-speed circuits. The result of this effort is the family of Low Inductance Chip Arrays (LICA®) capacitors. LICA® uses alternative current paths minimizing the mutual inductance factor of the electrodes (Figure 5). As shown in Figure 6, the charging current flowing out of the positive plate returns in the opposite direction along adjacent negative plates. This minimizes the mutual inductance.

The very low inductance of the LICA® capacitor stems from the short aspect ratio of the electrodes, the arrangement of the tabs so as to cancel inductance, and the vertical aspect of the electrodes to the mounting surface.

Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self-inductance of the electrodes. The self-inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further.

The inductance of this arrangement is less than 45pH, causing the self-resonance to be above 50Mhz for the same popular 100nF capacitance. As stated earlier the inductance of the component is just one half of the total inductance equation. When a capacitor is mounted on a board, lead lengths and board lines are other major sources of inductance. This inductance must be minimized to obtain good decoupling performance.

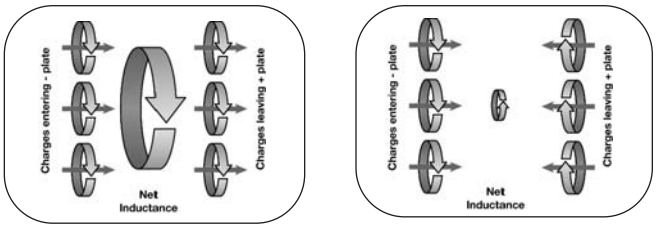

Figure 5. Net Inductance from Design

In the standard Multilayer capacitor, the charge currents entering and leaving the capacitor create complementary flux fields, so the net inductance is greater. On the right however, if the design permits the currents to be opposed, there is a net cancellation and inductance is lower.

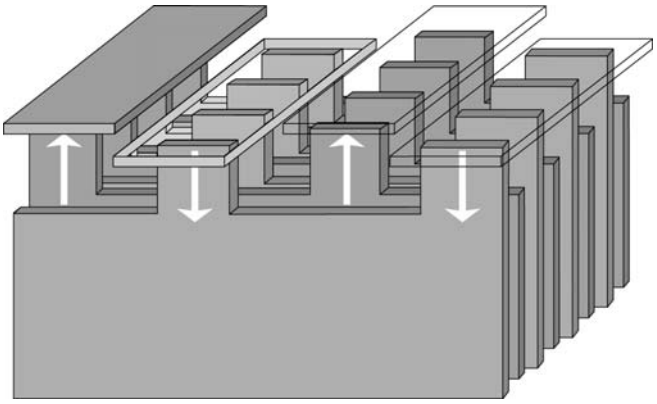

Figure 6. LICA®'s Electrode/Termination Construction

The current path is minimized – this reduces self-inductance. Current flowing out of the positive plate, returns in the opposite direction along the adjacent negative plate - this reduces the mutual inductance.

To lower mounted inductance LICA® utilizes flip-chip technology. Figure 7 shows a cross section of a bumped chip. The use of this C4 technology allows the designer to minimize loop inductance further by utilizing via-in-pad technology.

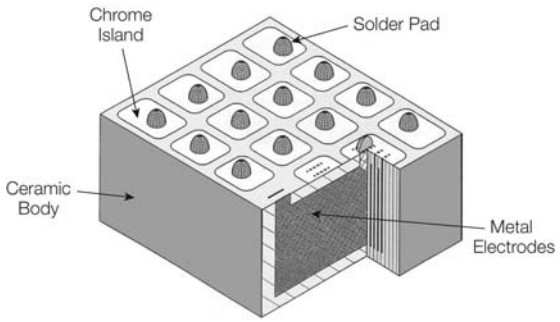

Figure 7. Cross Section of LICA® Chip

Mounting

The terminations on LICA® devices need to provide interconnections between the part and the substrate that have low resistance and low inductance, as well as adequate mechanical strength. Other factors in the selection of an interconnection technique include interconnect density, reliability, thermal performance, corrosion behavior, re-workability, turnaround, cost and manufacturing capability.

Controlled collapse chip connections (C4) is the most popular scheme used with the LICA® family. Developed in the early 1960s C4 has a long history of providing reliable, low inductance terminations using the minimum of real estate. The process AVX follows to bump a LICA® part begins by depositing several layers of metals onto the ceramic surface. These metals form an interconnection between the ceramic part and the solder ball but also serve to limit the spread of the solder on the surface of the chip, hence it is referred to as the ball limiting metallurgy (BLM). The final deposited layer is a lead-tin solder that is evaporated onto the BLM. The deposited solder is then reflowed at 380ºC in a reducing atmosphere.

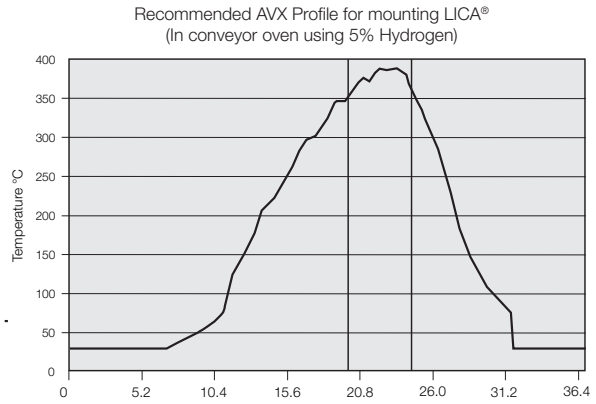

Figure 8. Typical Reflow Profile for LICA® Capacitor

Turning the part upside down, aligning it with the use of split optics and joining it to the mating surface makes the interconnection between the part and substrate. The use of tack flux keeps the part in place. Finally the assembly is placed into a reflow oven where the final electrical connections are made. An added advantage to C4 technology is the ability to self-align a part that is placed off center as long as the balls are placed on the pads of the substrate. AVX offers the LICA® family of capacitors with or without C4 solder balls to meet your processing needs.

The reliability of C4 mounting can be further enhanced with the use of standard flip chip underfills. The use of underfill significantly reduces solder ball stresses caused by different CTE's of joined materials. As always, consult with the underfill manufacturer for any process notes. An additional process note is to limit the meniscus from being more than ½ the height of the LICA® capacitor. This can be a problem since the capacitor is quite often located very close to other components.

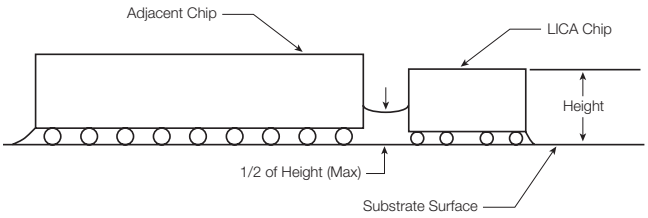

Figure 9

Summary

Summary

With the increase in circuit speeds and the concurrent continued miniaturization of circuitry a very different ceramic capacitor is demanded. The LICA® capacitor fills the void with a device that has very low mounted inductance and is efficiently designed to use little space. Unlike many other new components LICA® comes with many years of experience and a demonstrated history of manufacturing and reliability.

Characteristic	Ceramic Only	With Platinum Electrodes
Ageing		1.3%/Decade @ 25ºC
Thermal Conductivity	4.5 watts/meter ºK	
Heat Capacity	600 Joules/Kg	
Specific Heat	0.143 cal./gm	
Density	6.4 g/cc	
Thermal Diffusivity	0.009 cm^2/sec	
K1C Fracture Toughness	0.9 Mpa m	0.5 Mpa m
Young's Modulus	140 Gpa	
Fracture Strength	110 Mpa	
Thermal Coefficient Of Expansion	8.5ppm/ºC (25º-125ºC) 10.7ppm/ºC (25º-385ºC)	
Poisson's Ratio	.25-.33	
Vickers Hardness		750 Kg/mm^2
Dielectric Constant		5,500 (no bias, 25ºC) 8,000 (no bias, 55ºC)
Rated Field Strength		6 v/micron, 150 v/mil
DF		15% Max @ 25ºC
Maximum Pick & Place Forces		4.5 Newton's – Static 7.0 Newton's – Dynamic
DC Resistance		0.2Ω
IR (Minimum @ 25ºC)		2.0 Megaohms
Dielectric Breakdown, Min		500 Volts
Inductance (Design Dependent)		15 to 45pH
Frequency of Operation		DC to 5 Gigahertz
Ambient Temp Range		-55º to 125ºC

Typical Properties for LICA® family of Capacitors

With the increase in circuit speeds and the concurrent

APPLICATION NOTES

Storage

Good solderability is maintained for at least twenty four months provided the components are stored in their "as received" packaging at less than 40ºC and as dry as possible (not to exceed 70% RH).

Handling

LICA® ceramic capacitors should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of tweezers and vacuum pick-ups is strongly recommended for individual components. Tape and reeled components provide the ideal medium for direct presentation to the placement machine. Any mechanical shock should be minimized during handling.

Preheat

It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4ºC/second and a target figure of 2ºC/sec is recommended.

Cooling

Natural cooling in air is preferred, as this minimized stresses within the soldered joint. When forced air-cooling is used, cooling rate should not exceed 4ºC/second. Quenching is not recommended but if used, maximum temperature differentials should be observed according to the preheat conditions above.

Cleaning

Flux residues may be hygroscopic or acidic and must be removed. LICA® capacitors are acceptable for use with all of the solvents described in specifications MIL-STD-202 and EIA-RS-198. Alcohol based solvents are acceptable and properly controlled water cleaning systems are also acceptable. Many other solvents have been proven successful, and most solvents that are acceptable to other components on circuit assemblies are equally acceptable for use with ceramic capacitors.

PCB Board Design

To avoid many of the handling problems, AVX recommends that LICA® capacitors be located at least 0.2" away from the nearest edge of board. If this is not possible, AVX recommends that the panel be routed along the cut line, adjacent to where the capacitor is located.

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