

TECHNICAL PAPER

Introduction to Choosing MLC Capacitors for Bypass/Decoupling Applications

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Abstract

Methods to ensure signal integrity using decoupling capacitors have been the topic of many papers in the past as well as in the present. One can find equally many methods of decoupling as well. This paper will illustrate one of these established methods and introduce it in a theoretical sense using the most simplistic of terms. The paper will also describe the methods of the past (in slow speed systems) and the practices of the present (in high speed systems).

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Introduction

There have been numerous papers and articles published on the subject of *bypass/decoupling* methods to achieve *signal integrity*. The purpose and arrangement of this paper is to pull together the ideas from these various technical articles, the intent being a quick introductory guide to decoupling methods. It is meant to be a one-stop guide to define, establish the need, and illustrate a method in the science of decoupling. It should act as an introduction to a novice signal integrity or EMC designers who are looking to choose a Multilayer Ceramic Capacitor (MLC) for a bypass/decoupling (hereafter “decoupling”) application.

Definitions

Decoupling is a means of overcoming physical and time constraints found usually in a Power Distribution System (PDS) of a digital circuit [2]. Simply put, *decoupling* reduces switching noise in the PDS. Many times it is mistakenly referred to as *filtering*. These are two different applications and although a filtering circuit may perform decoupling, it is not optimally designed for that application. The same is true of a decoupling circuit. It may perform filtering, but it

was not designed to perform this specific function in a prime manner. Decoupling may be seen as a two terminal application and filtering as a three or four terminal application (Figure 1). *Decoupling* delivers energy to a specific point and *filtering* (typically an EMI solution) modifies a signal along a path.

The Need for Decoupling

As stated earlier, decoupling reduces noise in the PDS. Electrical noise can be caused in a number of different ways. In RF circuitry, oscillators and amplifier circuits generate this noise. In the digital environment, the switching integrated circuits, power supplies and regulators mainly generate this noise. This noise can be thought of as voltage ripple in the PDS. At a given current, I , this ripple voltage or the voltage drop (across an *ideal* capacitor) can be described by Equation (3):

$$I = C \frac{dV}{dt} \quad (1)$$

$$\frac{dV}{dt} = \frac{I}{C} \quad (2)$$

$$V = \frac{I}{\omega C} \quad (3)$$

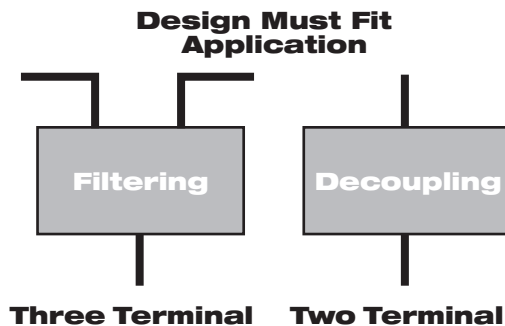


Figure 1: Types vs. Application

Equation (3) states that a current draw, I , leads to a voltage drop, V . As in most CMOS circuitry, the IC chip only draws current when the transistors are *switching*, and only a leakage current during the “0” or “1” state. This means that when the IC switches, it draws current; therefore it results in a voltage drop leading to ripple noise in the power distribution system (PDS). Furthermore, with increased processor speeds, the ripple noise is much greater since more logic states draw current, simultaneously.

Whether on the power and ground planes or the signal lines themselves, this ripple or interference can wreak havoc with the operation of the system. It can also cause radiated emissions. How it does this is very simple. The logic circuit may be seen as one of two possible states. On or off, true or false, high or low, whatever logic interpretation is used, it is *one* of two states. The setting and detection of these levels is achieved with solid-state switches that usually set and sense one state, and assume the other state is not set. There is a window of acceptance for this one state that is usually given as a percentage of the nominal. Moving near the minimum level creates some degree of uncertainty (Figure 2). There is a random determination of this signal as true or false. If a high frequency noise were then added to this set state, the degree of uncertainty increases as the level may move above and below the minimum required. The net effect is errors [2].

The main objective of *signal integrity* is to reduce these errors. In plain terms, signal integrity is having clean “0”s and “1”s for the logic states. To achieve signal integrity, decoupling methods are used. Decoupling methods (when properly applied) reduce the errors, by reducing the ripple noise in the PDS.

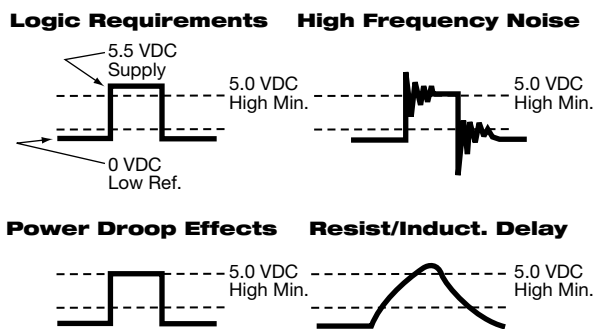


Figure 2: Logic Requirements and Error Conditions

Using decoupling capacitors is one of the most common, efficient and relatively inexpensive ways to achieve signal integrity. This is obvious from Equation (3). It states that (at a given I) an increase in C results in a reduction in V . Simply, merely increase the capacitance to get less ripple voltage (when the IC draws the current). The decoupling capacitor acts as a reservoir of energy located near the point of requirement. It delivers energy independent of the power supply during

the quick burst period, with enough reserves to maintain the required voltage level.

Return to REALity

As microprocessor clock speeds increase, what seemed to be an ideal capacitor can no longer be considered as such. A *real* capacitor can be modeled as a simple series RLC circuit as shown in Figure 3.

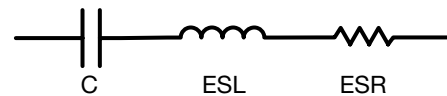


Figure 3: Equivalent Series Model for a Ceramic Capacitor

This is a distributed model approach, rather than a lumped model. The magnitude of the impedance of this series model is given as

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2} \quad (4)$$

where

$$\omega = 2\pi f \quad (5)$$

The Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) are the parasitics of the *real* capacitor [4]. This impedance, when plotted with frequency gives the graph a “V” shape as shown in Figure 4 [3]. AVX Corporation offers both web-based and stand alone software called SpiCAP to help model impedance vs. frequency response of MLC decoupling capacitors.

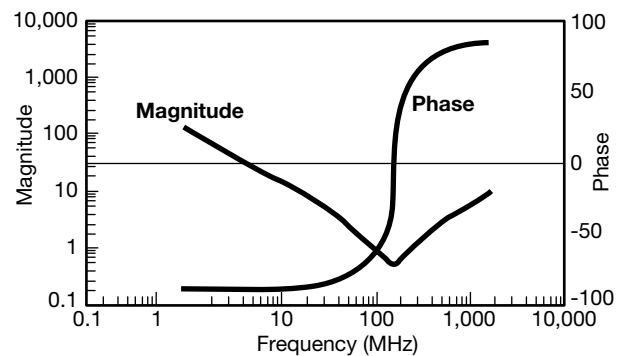


Figure 4: Typical Impedance and Phase for a 1000 pF Ceramic Capacitor

The left side of the “V” is the Capacitive Reactance portion of the impedance curve and is given as

$$X_c = \frac{I}{\omega C} \quad (6)$$

The right side of the “V” is the Inductive Reactance portion of the impedance curve and is given as

$$X_L = \omega ESL \quad (7)$$

The frequency where these two reactances are equal and cancel each other (at the bottom of the “V”) is the Resonant Frequency of the capacitor and is given as

$$f_{res} = \frac{1}{2\pi\sqrt{ESL \cdot C}} \quad (8)$$

It is at this resonant frequency where the ceramic capacitors reach their minimum impedance.

Those Annoying Parasites

In the early days of electronics, the inductive portion of the impedance, that due to the parasitic inductance of the capacitors, did not play a major role in decoupling applications. As technology advances with increasing clock speeds, however, the operating frequencies hover well into the inductive portion of the frequency range of these *real* ceramic capacitors. One can visualize this inductive behavior of the capacitor as a physical constraint that reduces the capacitor’s capability to deliver the quick bursts of energy to the switching IC (at higher frequencies).

Now, let’s qualitatively examine the effects of ESL on digital PDS. The voltage and inductance is related by the following equations:

$$V = L \frac{dI}{dt} \quad (9)$$

$$V = ESL \frac{dI}{dt} \quad (10)$$

$$V = \omega ESL \cdot I \quad (11)$$

Equation (9) says that a change in the current, I , will cause a voltage drop, V , in the PDS. Again, as in most CMOS circuitry, the IC chip draws current when the transistors are switching. This means that when the IC switches, there is a change in current, resulting in a voltage drop leading to ripples in the PDS. (Note: This holds true more so at higher frequencies ω or at shorter dt .) Again, it was illustrated earlier that any ripple in the PDS is a cause for errors. To reduce these errors at high frequencies, it is critical to use decoupling capacitors with the *lowest* ESL possible. This is clear from Equation (11), which states that (at a given ωI) a *reduction in ESL* results in a *reduction in V*, or ripple, in the PDS when the IC is switching.

Up to this point, the effect of ESL on the PDS has been shown, but what about ESR? In order to effectively decouple a PDS, it is necessary to use capacitors with the *lowest* ESR possible (at *any* frequency). For example, examine the effects of ESR at *lower frequency* regime. To explain, this *real* parasitic ESR term is introduced to Equation (3) and rewritten as

$$V = \frac{I}{\omega C} + I \cdot ESR \quad (12)$$

This means that the ESR term does *not* allow the voltage drop, V , to go away even if one increases the capacitance. In the *real world*, one must *increase capacitance* and *decrease ESR* in order to decrease the ripple noise in the PDS.

Incidentally, Equations (3) and (12) state that at higher frequencies, high capacitance does little to reduce the voltage drop (ignore the ESR term for a moment). Instead, Equation (11) tells us that at higher frequencies, reducing the inductance is more effective than increasing the capacitance.

A Basic Decoupling Methodology

There are many ways to decouple when designing a power distribution system. One of these methods is to identify a target impedance to be met across a *broad frequency range* and specify components to meet that impedance [1]. Given the voltage and power consumed, the

current is calculated from Ohm's law. Assuming that only a small percentage of the power supply voltage (i.e. 5%) is allowed as ripple voltage, target impedance for the PDS is calculated.

$$Z_{target} = \frac{\text{Allowed Ripple Voltage}}{I} \quad (13)$$

The target impedance must be met not only at DC, but also at *all frequencies* where current transients exist. Figure 5 shows the target impedance vs. frequency for a modern CMOS computer system. Several major components are used to meet this target impedance over the

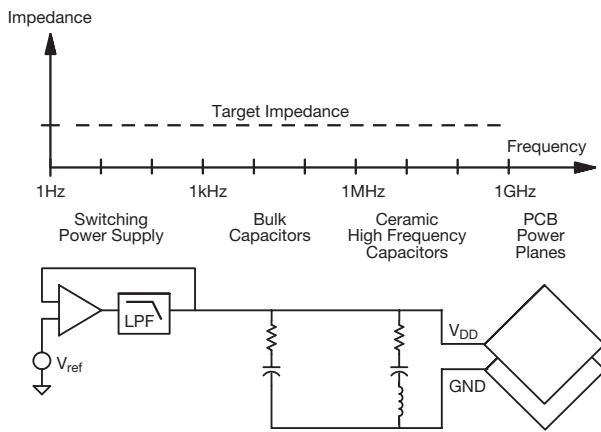


Figure 5: Flat Target Impedance vs. Frequency is Met by Using a Complex System of PDS Components

frequency range. The voltage regulator module (VRM) is effective up to about 1 kHz. Bulk capacitors supply current and maintain a low PDS impedance from 1 kHz to 1 MHz. High frequency ceramic capacitors maintain the PDS impedance from 1 MHz to 1 GHz. The inter-plane capacitance and the impedance of the printed circuit board power planes are important above 1 GHz.

This paper will focus on how to properly choose decoupling capacitors to meet the target impedance in the frequency range from 1 MHz to above 1 GHz. First, a method of choosing decoupling capacitors at *low* frequency decoupling will be shown. This will be followed by a discussion on choosing low inductance capacitors for *high* frequency decoupling.

Low Frequency Decoupling

It has been demonstrated (through Equations 11 and 12) that at *lower frequencies* (tens of MHz), high capacitance (coupled with lower ESR) more so than low inductance helps to reduce the ripple noise. The amount of capacitance needed to reduce the ripple voltage at a specific frequency is given by

$$C = I \frac{dt}{dV} \quad (14)$$

where dt equals the *slowest* rise time (low frequency) of a transient current. Suppose there is a 20 amp current transient, the VRM responds in 15 μ Sec, and the PDS must remain within 5% of a 1.8V power supply. The amount of bulk capacitance required is estimated by hand calculations:

$$C = I \frac{dt}{dV} = 20A \frac{15\mu\text{Sec}}{1.8V * 0.05} = 3333\mu\text{F} \quad (15)$$

Indeed, it would be impossible to find a 3333 μ F ceramic capacitor. The designer should find a suitable capacitor and place many of them in parallel to achieve this capacitance and the target impedance calculated earlier. (The effects of placing parallel capacitors will be discussed later.)

The ESL of the chosen capacitor for this application should not play a major role in decoupling, but the designer should seek the lowest possible value since it will lower the impedance over a broad frequency range. This will help reduce the number of decoupling capacitors on a board.

High Frequency Decoupling

At *higher frequencies* (hundreds of MHz), decoupling is more effective with reduced parasitic inductance than with higher capacitance (certainly, seek as high capacitance as much as possible). This is clear from Equations (11) and (12). The maximum amount of inductance allowed to minimize the ripple voltage is given by

$$L = V \frac{dt}{dI} \quad (16)$$

where dt is the *fastest* rise time of a transient current. Suppose there is a 20 amp current

transient with a rise time of 1 nSec, and the PDS must remain within 5% of a 1.8V power supply. The amount of inductance allowed is estimated by hand calculations:

$$L = V \frac{dt}{dI} = 1.8V * 0.05 \frac{1nSec}{20A} = 4.5pH \quad (17)$$

Today, it is difficult if not impossible to find a surface mount ceramic capacitor with an ESL of 4.5 pH. Considering that this is a mounted inductance, it further sets the inductance requirement of the capacitor to a lower value. Again, the designer would achieve this inductance and the target impedance by first choosing a capacitor with the lowest parasitic inductance. (The capacitance of the chosen component should not play a major role in decoupling at the higher frequencies, but one should seek the highest possible value for a given low ESL, since it will lower the impedance over a broad frequency range.) A sufficient quantity of these low inductance capacitors should be placed in parallel. This often requires the designer to place more chips than the board space allows. Thus, it is critical to use capacitors with very low inductance to reduce quantity, board space, and cost.

Most often, it is difficult to find a conventional (rectangular) surface mount capacitor with low parasitic inductance. An effective way to lower the inductance of a rectangular chip is to modify the design to terminate along the length of the chip as shown in Figure 6 [5]. In some instances, this technique has reduced the ESL by 50%. An AVX 0612 LICC (Low Inductance Chip Capacitor) has an ESL rating of about 550 pH while a similar package 1206 capacitor has about 1250 pH of inductance when measured. The impedance of these two chips (both 0.1 μF) is shown in Figure 7.



Figure 6: 1206 vs. 0612 LICC

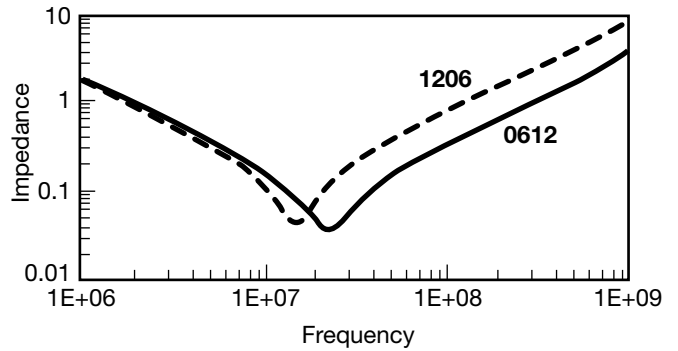


Figure 7: Impedance Comparison of 1206 vs. 0612 LICC

Another method that has shown itself to be effective in lowering the inductance value of the capacitors is multiple terminations. One device on the market today is the Inter-Digitated Capacitor (IDC). This is an eight terminal component that contains one capacitor (Figure 8). This non-polar device is connected to the power/ground planes by alternating each termination to the individual planes. These devices are available at AVX in both 0612 and 0508 versions. An AVX 0612 IDC has an ESL rating of approximately 175 pH while an AVX 0508 IDC has approximately 110 pH of inductance when measured.

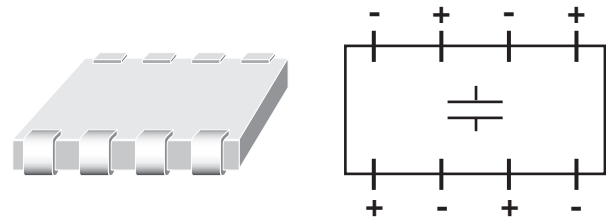


Figure 8: AVX IDC

Decoupling at a Particular Frequency

At this point, one should have a set of capacitors that covers the *highest* and the *lowest* frequency components. But, the target impedance must be met over the *entire* frequency range of concern for improved product performance. To meet a target impedance at a *particular frequency*, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency (Equation 8), and have an impedance that is equal to its ESR. This takes advantage of the resonance because ceramic capacitors reach their *minimum impedance* at their resonant frequency. Then, a

sufficient number of those capacitors are placed in *parallel* so that the parallel ESRs approach the desired target impedance.

Now, the designer may wonder, how many capacitors must be placed in parallel? That can be answered by the following equations:

$$C_{total} = n \cdot C \quad (18)$$

$$L_{total} = \frac{L}{n} \quad (19)$$

$$ESR_{total} = \frac{ESR}{n} \quad (20)$$

where n = number of capacitors in parallel. Using this, Equation (4) can be rewritten as the following:

$$|Z| = \sqrt{\left(\frac{ESR}{n}\right)^2 + \left(\frac{\omega ESL}{n} - \frac{1}{\omega n C}\right)^2} \quad (21)$$

Figure 9 shows the effect of placing several identical capacitors in parallel. The impedance is reduced by a factor of 2 every time the number of capacitors is doubled. There is a diminishing

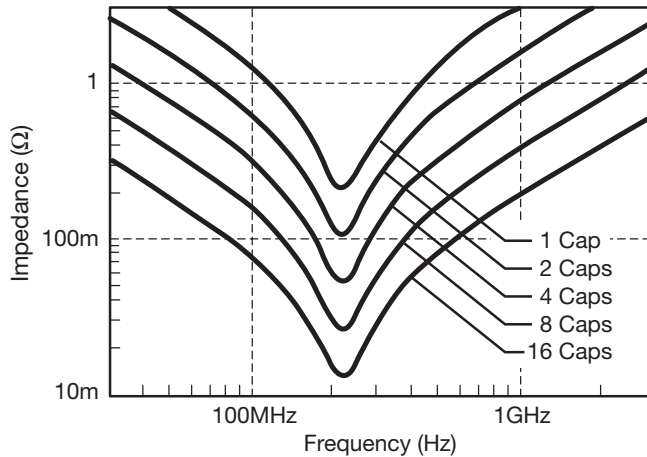


Figure 9: Effect of Parallel Capacitors on Impedance

return with each additional capacitor. It is desirable to start with low ESR capacitors in order to minimize the number of capacitors required to meet a target impedance. One should immediately notice from Figure 9 that as additional identical capacitors are placed in

parallel, the resonance frequency does *not* shift. This is clearly the case after one examines the equation for the resonant frequency when adjusted for the parallel capacitors:

$$f_{res} = \frac{1}{2\pi \sqrt{\frac{ESL}{n} \cdot nC}} = \frac{1}{2\pi \sqrt{ESL \cdot C}} \quad (22)$$

Equation (22) is exactly the same as Equation (8) shown earlier. In summary, as more of the same capacitors are placed in parallel, this effectively increases capacitance, reduces parasitic inductance, and reduces ESR. This results in a decrease in capacitive and inductive reactances without any changes in the resonant frequency, according to Equations (6), (7) and (8).

Caution must be taken when placing *different* values of capacitors in parallel, as a designer undoubtedly must do. When capacitors of different values are placed in parallel, they produce an unwanted *anti-resonance* [1]. It is a peaking between the two *resonances* of two capacitor values. The peak is higher than the impedance of either capacitor by itself (Figure 10). The peak is associated with the circuit that is formed after one capacitor has gone *inductive* and the other capacitor is still *capacitive*, the classic parallel LC tank circuit. The most effective way to reduce the height of the anti-resonance is to minimize inductance. Large anti-resonant peaks develop when low ESR capacitors are placed on inductive pads. High inductance and low resistance make a high Q circuit where the Q is given by the following equation

$$Q = \frac{X_L}{ESR} \quad (23)$$

and at *resonance*, this becomes

$$Q = \frac{\sqrt{ESL}}{ESR} \quad (24)$$

High Q circuits make the troughs *deeper* and peaks *higher*. To achieve a *moderate* Q circuit, one must minimize ESL rather than increasing the ESR, since it was already demonstrated that ESR always creates a ripple voltage as shown in Equation (12). Furthermore, reducing the ESL

will help avoid any unwanted resonances between the board power plane capacitance and the decoupling capacitor inductance. A good rule of thumb is a Q of 2 to 5. For Q of more than 5, the anti-resonance peaks are not manageable.

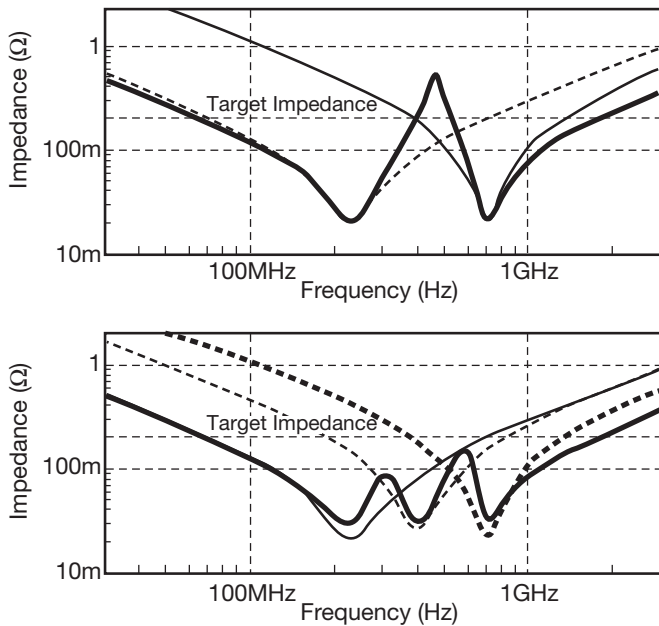


Figure 10: Anti-Resonance Effects
Bottom Graph Shows 3 Values of Capacitors
vs. 2 Values of the Same Quantity of Capacitors

Circuit with Q less than 2 take an excessive number of capacitors to achieve low PDS impedance. The anti-resonance also becomes high if large gaps exist in capacitance value. Anti-resonances are effectively managed by using low inductance capacitors and many values of capacitors (Figure 10).

Mounted Inductance

The ESLs mentioned so far have only been limited to the parasitic inductance of the chip package itself. However, this is only a small portion of the total inductance that impairs the overall PDS performance. The ESL of the chip is part of a much greater inductance developed within the current loop of the chip-pad-trace structure on the board (Figure 11). The inductance associated with traces connecting a decoupling capacitor to the power rails is significantly higher than the parasitic inductance of the capacitor itself. A good rule of thumb is 10nH/in. for trace inductance [6]. High frequency decoupling performance of a low inductance

capacitor (such as AVX LICC) is considerably reduced when mounted on a high inductance mounting structure (Figure 11). In the early 1990's, decoupling capacitor inductance was dominated by pad layout.

For today's high frequency decoupling applications, it is crucial to minimize the loop inductance. One way to minimize the loop inductance (in addition to using low inductance capacitors) is to reduce the size of the loop area. For the layout shown in Figure 11, running the power rails close together, even to the point where the power rails run below the IC can

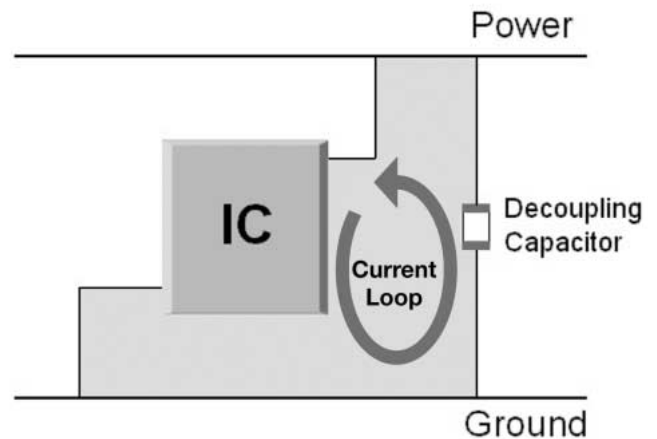


Figure 11: Large Current Loop Generated by Poor Placement of Decoupling Capacitor

reduce the loop area. However, for high frequency decoupling, the performance is still limited by the inductance of the traces and the power rails. The loop inductance can be further reduced by the use of via-in-pad, though costly, that makes use of the very low inductance nature of power and ground planes. Via-in-pad is no exception; the designer should still strive to reduce the current loop. The current loop is minimized by bringing the vias close together and reducing the height of the vias and capacitor. A small trace between the pads and vias adds an

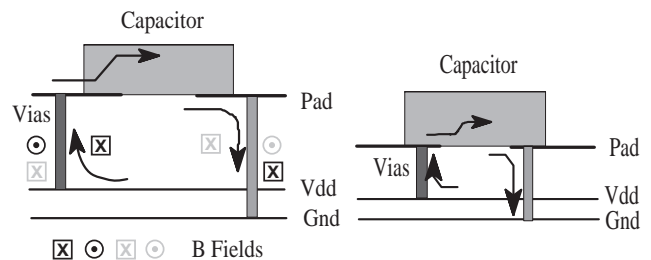


Figure 12: Inductance Developed in Current Loops

enormous amount of inductance. Again, a good rule of thumb is 10nH/in. for trace inductance. Vias should be brought as close together as possible to minimize inductance (Figure 12 and 13). The limiting factors are manufacturing issues at PCB fabrication and component assembly [1].

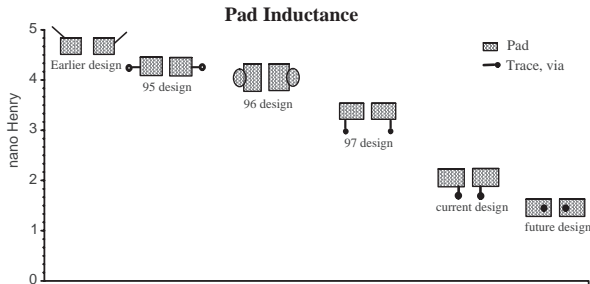


Figure 13: Decoupling Capacitor Pad Design Progression

With optimum pad design, the dominant inductance is associated with via and capacitor height. Vias are a natural inductor in the shape of a hollow or a solid tube [5]. The value of via inductance is directly proportional to the length and the diameter of the tube. Figure 14 shows the inductance of a via for a variety of lengths and diameters. Obviously the best method for keeping this number down is to keep the power and ground planes as close to the top/bottom of the PCB as possible. While this is not always prudent, it is very common to find ground planes on top and bottom, with the power plane in the middle of the PCB. As shown in Figure 14, running a decoupling capacitor via (8 mil diameter) all the way through a 60 mil circuit board can add 1nH of inductance.

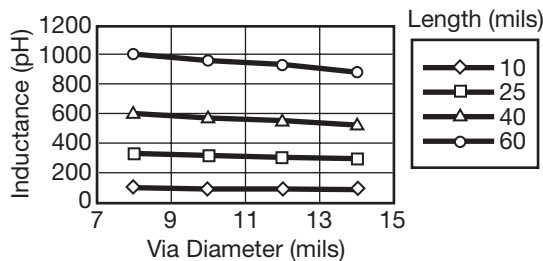


Figure 14: Different Vias and Its Associated Inductance

The vertical distance traversed by the current increases the size of the loop and therefore the inductance. The effect of capacitor height with respect to the current path is shown in Figure 15

and Table I. Optimizing the pad design and minimizing the distance from the top of the capacitor to the Power/Ground plane pair, the inductance associated with the decoupling capacitor is minimized [1].

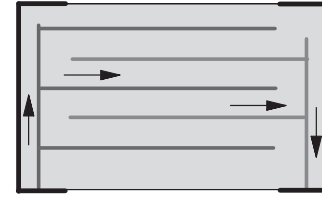


Figure 15: Current Path within a Multilayer Ceramic Capacitor

Thickness (mils)	Inductance (pH)
20	300
30	450
40	600
50	700

Table I: Inductance Contribution from Chip Height

Basic Decoupling Recommendations

- 1) Find a target impedance of the PDS by using Equation (13)
- 2) Find the necessary *bulk capacitance* for the lowest frequency component (slowest rise time) of the circuit by using Equation (14)
- 3) For bulk capacitors, choose capacitors with high capacitance with low ESR to reduce ripple voltages.
- 4) Find the maximum *allowable inductance* for the highest frequency component (fastest rise time) of the circuit by using Equation (16)
- 5) For high frequency decoupling, choose capacitors with the lowest ESL to reduce the number of capacitors needed in parallel to meet the target impedance.
- 6) For high frequency decoupling, choose capacitors with Q between 2 to 5 in order to minimize any unwanted anti-resonances.
- 7) When placing a given number of capacitors in parallel, use many values of capacitors rather

than just a few different values to minimize any unwanted anti-resonances.

8) Take advantage of the low impedance at resonant frequency to reduce the number of capacitors needed in parallel to meet the target impedance.

9) Reduce the mounted inductance by reducing the current loop area.

Conclusion

This paper summarized various papers and articles from the theoretical perspective of decoupling in the design of power distribution system. The terms *signal integrity* and *decoupling* were defined and the need for them has been shown. One method of using decoupling capacitors when designing a PDS has been illustrated. The need for high capacitance and low inductance capacitor has been demonstrated along with the generalized behavior of a real capacitor.

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