

# TECHNICAL PAPER

## PE Series Capacitors Decoupling and/or Filtering

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### **Abstract**

Decoupling is a means of eliminating or reducing those elements which restrict high speed operations. Filtering is driven by two considerations – emission and susceptance. The noise generated in high speed digital operations may need to be reduced, to achieve accepted levels of emission to prevent interference with other systems. Also, the system itself may have its distinct level of noise tolerance which would require filtering selected inputs to maintain integrity of the logic circuit operations.

The solution to a decoupling problem may assist filtering, and vice versa; but, the optimum solution to either is not the optimum solution for the other.

The *PE* devices were originally designed for filtering, and then were later designed for decoupling. The application defines the requirement and the optimum design.



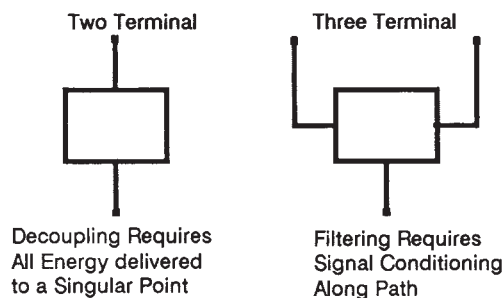
# PE SERIES CAPACITORS DECOUPLING AND/OR FILTERING

by John D. Prymak  
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## Decoupling vs. Filtering

This paper will deal with all aspects of power entry stabilization in that this activity relates to two distinct functional requirements - decoupling and filtering. Although many use these terms interchangeably, they are distinct and sometimes contradictory conditions.

Decoupling is a means of insuring energy transfer capabilities at or to a specific point or circuit node. Filtering relates to the conditioning of a signal along a path - with separate start and finish locations. Although good decoupling may preclude the requirement for filtering, filtering is not the primary consideration. Likewise, good filtering may include some decoupling, but it is not optimized for this task.



## Decoupling to Inhibit Noise Generation and Emission

Decoupling can be separated into three distinct categories: power supply decoupling (DC-DC converters), power entry decoupling and circuit level decoupling. Power supply and power entry are distinct in that the currents and voltages involved are so different. The circuit level could be looked at as a power entry to an individual IC. Within the IC there may possibly be separate decoupling required for distinct circuit elements within the IC - but they would be of the same approximate energy requirements (capacitance) and should be lumped as "circuit level".

In all cases, it is the function of the decoupling capacitor to deliver the quick burst of energy, within a specified time element, without generating a noise pulse or an apparent voltage droop.

Because of the inductance and resistance associated with the distance to the power supply or the inductance and resistance of the supply output, energy transfer directly from the supply would cause a "droop" in voltage apparent, or noise at the circuit level on the card in today's high speed logic circuitry. The required packet of energy is held in storage by the nearby, decoupling capacitor to supply quick energy transfers without generating noise or subsequent logic errors.

## Capacitor Filters to Reduce Noise Generated

The noise reduction is accomplished in a low-pass configuration. The purpose of the low-pass capacitive filter is to shunt the unwanted high frequency signals to ground. The capacitor offers an impedance path that is frequency dependent - as frequency increases, the impedance decreases.

The physical characteristics as well as means of connection have a significant effect on the performance of this circuit. A leaded capacitor connected from the signal line to ground is a simple low-pass filter circuit. The high frequency performance of this solution shows that this circuit is not purely capacitive, but inductive as well. It may not perform as expected.

There are no perfect components. There are some that are better than others, and some that are well beyond any discernible difference from "perfect" in specific applications. The parasitics in the capacitor itself are ESR (Effective Series Resistance) and ESL (Effective Series Inductance).

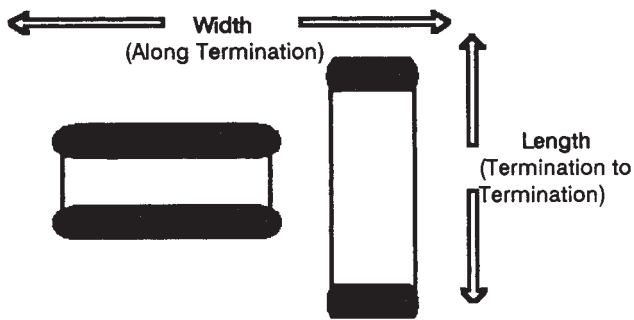


The noise reduction may be enhanced by designing a  $Pi$  or  $L$  type of filter; but, it must be pointed out that this type filter adds cost and space to the board while reducing the decoupling capability. Some experts have promoted these types of filters with the added condition of decreasing speed of the circuitry to reduce the decoupling requirements - I consider this a "head in the sand" solution.

## ESR Composition in MLCs

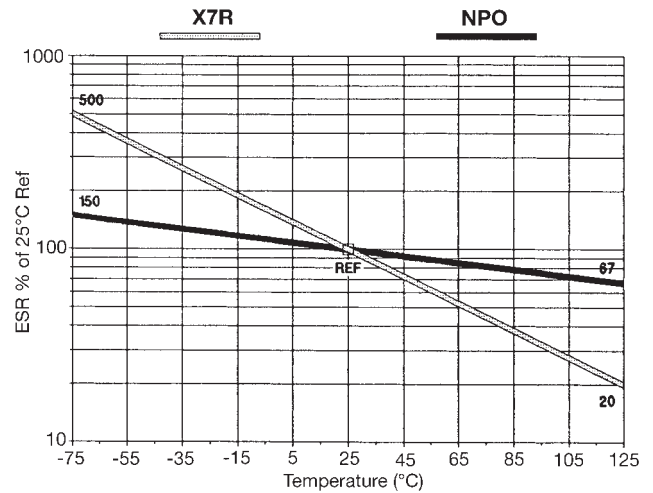
The resistive elements within the MLC (multi-layer ceramic) capacitor which contribute to ESR are the electrode plate resistance, termination material resistance, interface resistance at the electrode-termination junction, and dielectric resistance. The *termination resistance* is such a minor contributing factor that it will be ignored for the rest of this discussion.

The *plate* and *interface resistances* may be effected by changing the physical construction of the capacitor. Shorter and wider plates will decrease the plate resistance contribution. The wider plates will also increase the area of interface contact, thus reducing this resistive contribution. As a matter of convention, we refer to width as that dimension along the termination and length as that dimension between opposite terminations.



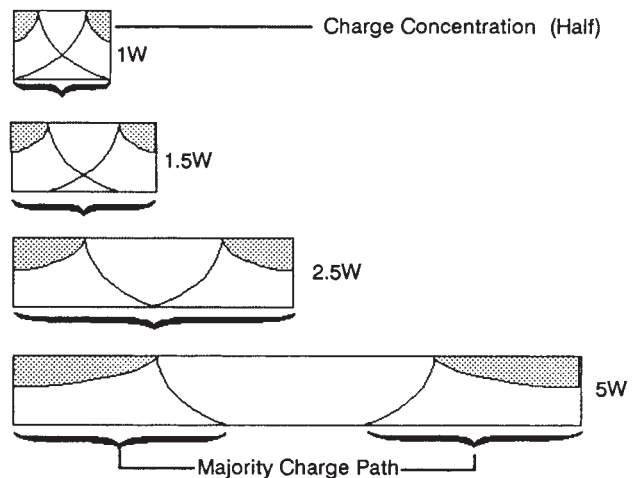
The effects of *dielectric resistance* is readily seen in the effect of temperature on ESR. As the kinetic energy of the molecules in the dielectric increase, the resistance to field support also decreases. (There is also an increase of the pressure of contact at the electrode-termination junction because of the expansion of these metals, further reducing overall ESR.) The *dielectric resistance* is also greatly effected by frequency - as frequency increases the time required for field support decreases and the efficiency of the dielectric increases. It will decrease to a point where it offers little contribution to overall ESR and is lost in dominance of the other factors. The *junction resistance* element is the easiest understood factor contributing to ESR changes in frequency. There is a high leakage capacitance at this junction that shunts more of the signal as frequency increases. The ESR actually decreases as frequency increases. After a point, this factor is negligible and "*skin effect*", associated with the plate conduction depth, starts to increase the overall ESR.

ESR vs. Temperature



## Low Inductance Designs

The ESL is dictated by signal restriction. If the path is narrow and long, the ESL is high. If the path were wider and shorter, the ESL would decrease. This is the approach followed in the design of the *SupraCap™* devices for switched mode power supply applications. There is a limit as to how much the aspect ratio can effectively reduce the inductance. One concern is dictated by practical considerations in mounting (tombstoning) and handling (all assembly equipment built for higher aspect ratios). Also, the aspect ratio does not eliminate the mutual inductance between the opposite charging plates. Charge concentration at the opposite corners from the termination corners still dictates that the currents are concentrated nearest these corners. After reaching some point, decreasing the aspect ratio has no noticeable effect on decreasing inductance.



The low inductance designs for *SupraCap™* are ideally suited for switch mode power supply input capacitance. These are fairly large devices (width max. 2") with peak current capabilities of thousands of

amps. In the higher frequency switchers (> 100 KHz) as input capacitors, they allow quick energy bursts without generating large noise ( $L \times di/dt$ ). Also, because their design requires a DIP lead attachment, they offer good filtering of noise generated in the solid state switching circuitry. They have capacitance capabilities from 1  $\mu$ Fd to 400  $\mu$ Fd in X7R, and to 1000  $\mu$ Fd in Z5U/X7V. The inductance for these devices is from 1.7 nH to 0.4 nH, depending on style.

Using the same technology on the circuit level is a family of devices designated as *L-Bond*™ chips. These consist of 0508, 0510, and 0612 devices. The inductance ranges 0.7, 0.6, and 0.6 nH, respectively. They were designed with a low profile (< 20mils) in

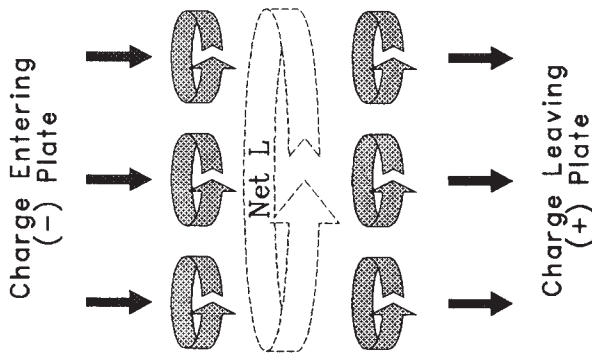


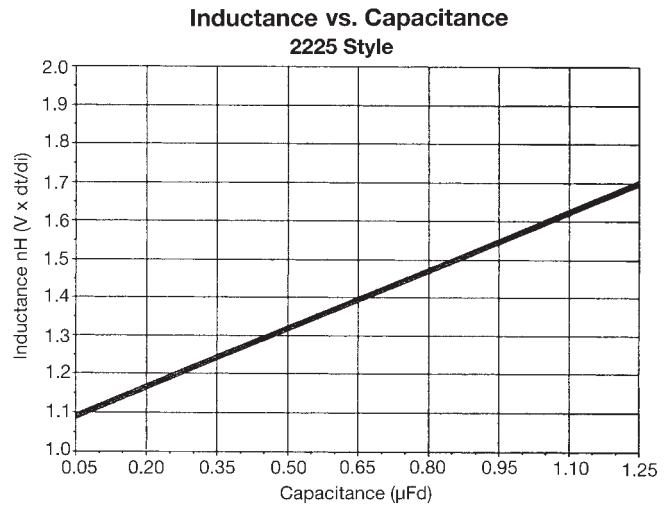
Figure 1. Mutual Inductive Coupling MLC Parallel Plate Construction

mind to allow location within the IC package. The low aspect ratio highlights handling and surface mount considerations evident with the standard 0805, 1005, and 1206 sizes, but there are instances (sub micron designs) where they are the only device that is capable of performing in this application.

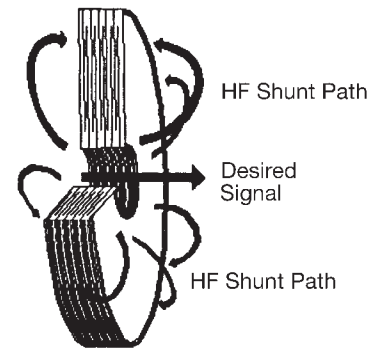
## PE Designs - Inductive Cancellation

If the path were made to be multidirectional, the ESL is again decreased. Figure 1 depicts the accumulation of inductance as found in the standard MLC design. It now becomes the physical dimensions and charge propagation path(s) of the capacitor which dictates its ESL.

Within a specific chip style, the ESL does vary with the capacitance. As the capacitance is increased, the cross sectional area increases. This effect of lowering the inductance is overridden by the increased inductance due to mutual coupling increase with an increase of plates. As the capacitance of a package is increased, the ESL also increases. The chart above shows how the inductance of a singular style varies with capacitance.



Discoidal Capacitor Multiple High Frequency Path



The discoidals efficiency in this area is readily seen as charges being fed in a multidirectional path while the PE device can be seen as being fed from two opposite directions with the subsequent shunt capacitance in opposite directions at 90° rotation from the feed path - negating a very large contribution to ESL as in Figure 2.

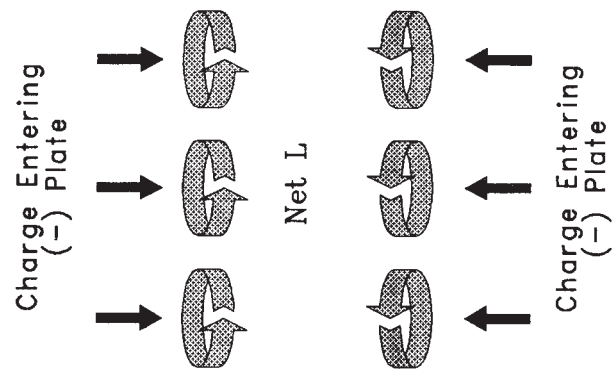


Figure 2. Inductive Cancellation PE Opposite Edge Plate Feed



## Parasitics and Type/Style

Getting back to filter applications, these parasitics inhibit the performance of the low pass filter, most noticeably at the higher frequencies. If leads are a part of the unit being used, the additional inductance and resistance of the leads negates the low impedance of the capacitance. If a chip were to be used, the physical dimensions of the package dictates the inductance and resistance capabilities.

Consider the data of Figure 3 representing the insertion loss for chips mounted on a substrate for multiple pin connectors. The predominant restriction in this application was the chip size. Maximum allowable was an 0805 (0.080" x 0.050") chip. The insertion loss increases dramatically to a maximum (38db @ 150MHz), then decreases back to a level

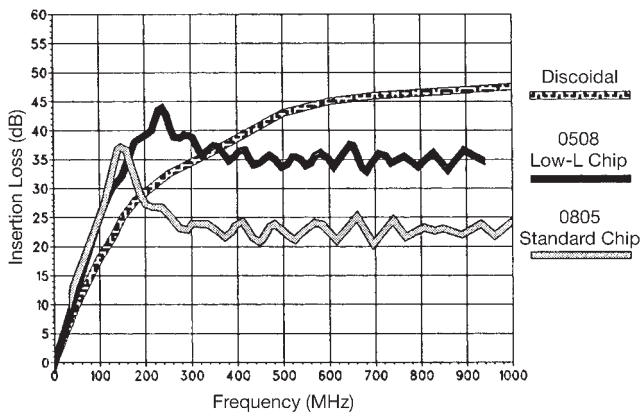


Figure 3. Insertion Loss Style Dependence

(< 25db) where it remains constant. By changing the size from 0805 to 0508 (0.050" x 0.080"), the shift in peak attenuation is to a higher frequency (@ 240MHz) with higher magnitudes in both peak (44db) and settled levels (< 38db) of attenuation. These are equal capacitances of the same effective and ceramic with only their aspect ratios effected.

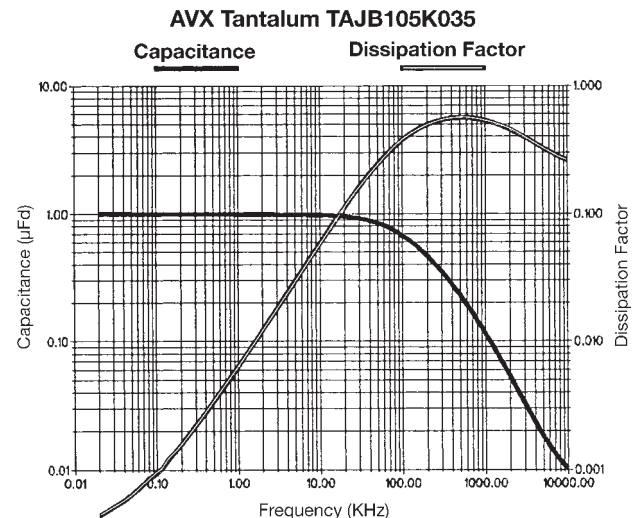
A comparison of these two chip styles with the discoidal design is also shown in Figure 3. The discoidal is a circular type capacitor with terminations at the inside and outside diameters as depicted in the previous diagram. The signal is fed through the center of the unit while the high frequency is allowed to propagate in all directions as it goes to ground. Again, this is not a perfect unit, but the discoidal and tubular ceramic capacitors are as close to the perfect or ideal as possible.

The ESL of the discoidal is so low, that even when the inductive element dominates, its impedance is extremely small and rises at a rate slightly higher than the load. The inductive effects of this device do

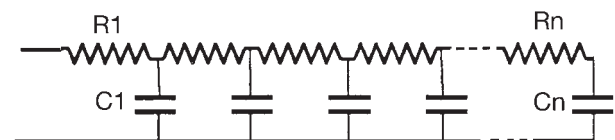
not begin to show up till well beyond a Gigahertz in frequency. In some cases, the point of "self-resonance" cannot readily be found on a 50 ohm system with less than 100db dynamic range ( $Z = 25 \times 10^{(db/20)} / (1 - 10^{(db/20)})$ ).

The type of capacitor also has some effect in its application. A Tantalum or electrolytic has poor high frequency performance due to its inherent physical composition. As frequency increases, the capacitance realized in the circuit decreases, because its resistive element is so high that the RC time constant of a portion of this type is too long to respond to a short time pulse.

The following graph highlights one manifestation of this problem. The capacitance plotted versus frequency shows a constantly decreasing magnitude. The resistive and inductive elements are so high, that they effectively isolate increasing portions of the total capacitance as the time period decreases below their time constants. The inductive element is now in series with an ever decreasing capacitance - resulting in a higher self-resonance point.



The equivalent circuit for these devices at high frequency, becomes an RC ladder type network terminated at two points. The response time is dependent upon the Resistive (and Inductive) elements which are fixed by material and construction.



$$\text{Time Constant 1} = R1 \times C1$$

$$\text{Time Constant n} = (R1 + R2 + R3 + R4 + R5... + Rn) \times Cn$$

Electrolytic and Tantalum  
"RC Network" Response

Figure 4 shows *apparent* capacitance to a constant current pulse which changes levels in 1 nS. The capacitance is calculated from the  $dv/dt$  (Capacitance =  $I \times dt/dv$ ) slope in response to a 200 mA constant current pulse. The  $dv/dt$  response of the electrolytic and tantalum capacitors reveal a decaying slope that is extremely steep at first (low capacitance) and stabilizing to a slope corresponding to its “*marked*” value, microseconds after pulse initiation. In response to a demand for a burst of energy, the energy is delivered at a much smaller rate until microseconds have passed; and then, the rate corresponding to the *marked* value of the capacitor is achieved.

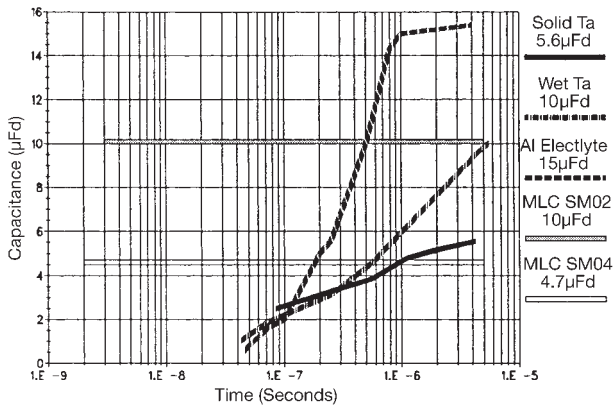


Figure 4. Capacitance as Measured from  $dv/dt$  Slope

In Figure 5, the insertion losses of various devices are shown. The Tantalum 5.6 Mfd capacitor is a radial leaded “tear-drop” device which is most popular in the power entry application. The MLC chips are a 1510 style, Z5U type of 1.3 Mfd, and, a 2225 style, X7R type of 1.0 Mfd. The PE device is a PE07 style, X7R type of 2.2 Mfd. All except the PE style (45db), show performance at 1 Gigahertz of less than 20 db insertion loss.

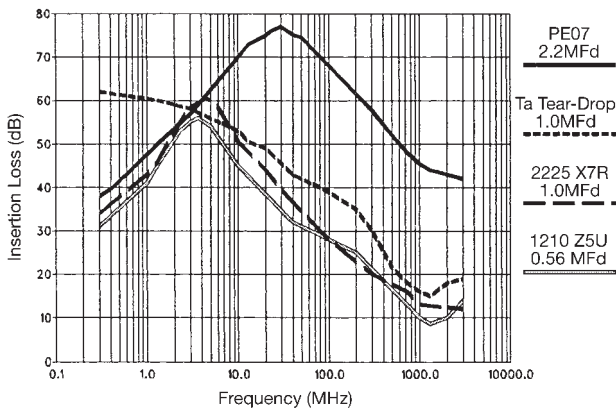


Figure 5. Insertion Loss

## Eliminating Parasitics in Filter Design

In all cases up to this point, the device is connected to shunt the load. The connection is a point of

restriction, therefore, it is a point of inductance. As shown in Figure 6, the shunt capacitor gives three nodes of high frequency impedance: 1) connection to line, 2) connection to ground, and, 3) internal parasitics.

The feed-through inductive capacitors as designed in the *PE*<sup>TM</sup> series of Power Entry Decoupling Capacitors are unique in that the shunt path to ground is inherent in extension of the signal path within a dielectric and offers a distributed capacitive shunt to ground unrestricted to a small finite connection. (For power supply filtering, the device may not be able to handle the bus current, and as such, it is connected as a shunt device with two points or areas of bus contact.)

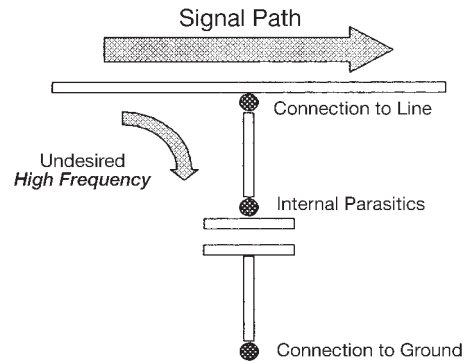


Figure 6. Shunt Capacitor Decoupling/Filtering Signal Line/Path Uninterrupted

Figure 7 depicts this serial configuration with two nodes of high frequency impedance: 1) internal parasitics, and, 2) connection to ground. These two nodes are greatly reduced because the aspect ratio for the high frequency path is so low and the termination contacts to ground have multiplied. Also, the path to ground for the “*noise*” is now in two possible directions that are 180° opposed to each other. The ESL is greatly reduced in this configuration. The

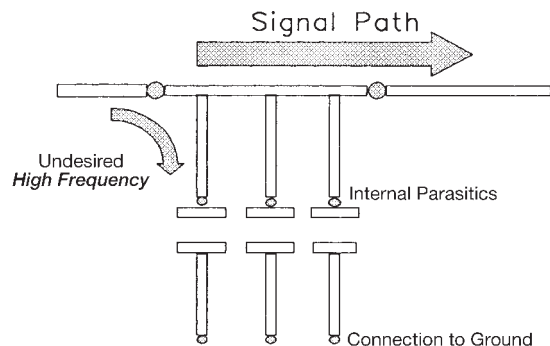


Figure 7. Power Entry Decoupling/Filtering (PE) Signal Line/Path Interrupted

points of maximum attenuation, or minimum impedance of the pass element occurs at its apparent self-resonant point. For the standard MLC chip designs, the self-resonant points of 3.3 MHz for the 0.56 Mfd and 4.2 MHz for the 1.0 Mfd result in ESL calculations of 4.2 nH and 1.4 nH, respectively. If the same analysis is applied to the PE07, 2.2 Mfd at 31 MHz, the ESL calculates to 12 pH.

This capacitor is built to connect within the signal line. The points of connection are part of the signal path and not the ground path. This additional impedance in the signal path is totally insignificant to the low frequency signals. In addition, since the units length contributes to the inductance in the signal path, both signal series inductance and ground impedance are effected in an enhanced mode in this unit.

Looking at the insertion loss for all style of the PE devices, the rate of loss is 6db per octave (20db per decade). This loss is in perfect agreement with the calculated loss of the ideal capacitor using Formula A.

$$db = 10 \times \log_{10} [(50 \times \text{Pi} \times \text{Freq} \times \text{Cap})^2 + 1]$$

Formula A

Figure 8 shows the decrease after peaking can be reduced somewhat in the very high frequencies, > 1 GHz, by terminating a ground *band* completely around the device. There is a capacitance from signal input to output which shunts the low pass configuration. The impedance of the low pass configuration in its ground path is critical. The resistance of this ground termination band is much lower than that of the internal electrode. This decreases the overall impedance to ground and increases the level of higher frequency insertion loss. Additional increases of very high frequency insertion

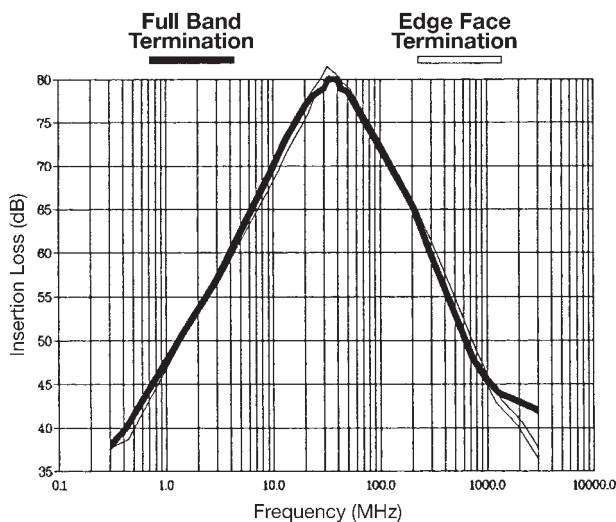


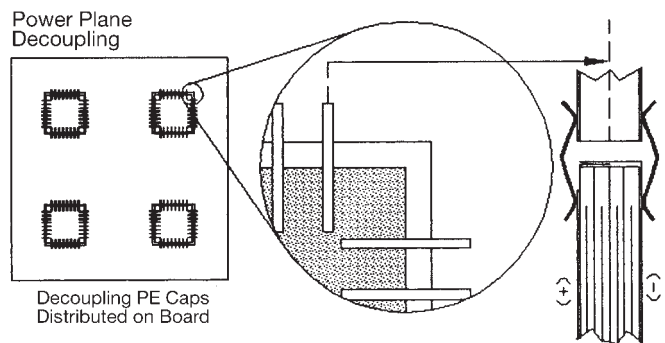
Figure 8. PE07  
Full Band vs. Edge Termination  
2.2 Mfd 50 WVDC

loss can be achieved by mounting the PE into the grounded chassis or bulkhead at the perimeter termination, but this is totally impractical for a surface mount application.

## Power Plane Decoupling

How does the design of the PE device effect its performance in decoupling? In a somewhat different approach, the PE designed for this application would require an aspect ratio very close to unity. Whereas the high aspect ratio (as seen by the signal to be attenuated) of the signal path and low aspect ratio of the ground plate, enhance its filtering performance, this has no beneficial contribution to a two-terminal requirement. As a matter of theory, the shortest distance between the opposite feed edges will afford the greatest inductive cancellation. Since there is no desire to reduce this maximum effort in either power or ground plate, the aspect ratio should be 1.

The contact from the capacitor plate to a power plane or ground plane is depicted in the following illustration. The PE device sits in a window in the circuit board, and perimeter contacts are made to both planes. Connection to the internal electrodes, which are now coplanar to the circuit board and termination faces, is accomplished by edge termination extending over opposite edges for each face (90° rotated for opposite terminations), or by means of blind holes or vias. These devices are then distributed throughout the board and the digital devices are connected directly to power and ground planes.



The PE signal path is maintained to afford cancellation by feeding from opposite directions. For larger capacitances in larger packages (~ 1" square), current density and inductive cancellation may be enhanced by making multiple vias or slots, distributed over the larger face of the larger devices. This affords greatest cancellation of inductances because it allows shorter distances between opposing currents. Smaller devices (~0.25" square) requires only that the

termination overlap three adjacent faces, with margins set to prevent shorting to the opposite termination.

## Multiple Line Filtering

The MLC has established itself well in filtering multiple lines using the planar array. This device is a monolithic arrangement of multiple, individual capacitors with a singular ground. Typical configurations shown in Figure 9, depict the rectangular and circular products offered as standard line items.

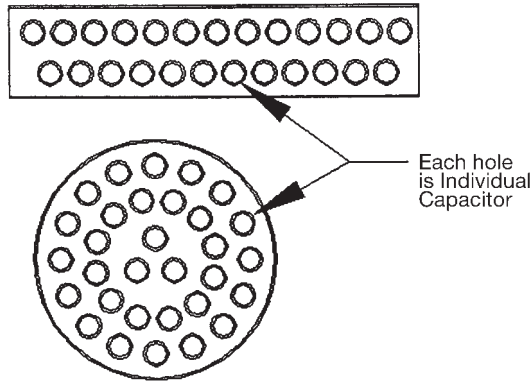


Figure 9. Rectangular and Circular Planar MLC Arrays

One of the problems with this device is in attaching multiple pins with a solder connection. All pins are to be done at one time and the MLC material demands utmost caution and care in process.

An alternative to this array would be in the use of a PE type or serpentine feed-thru array. Again, since the aspect ratio of the signal feed is required to be high for optimum conditioning, the serpentine path as

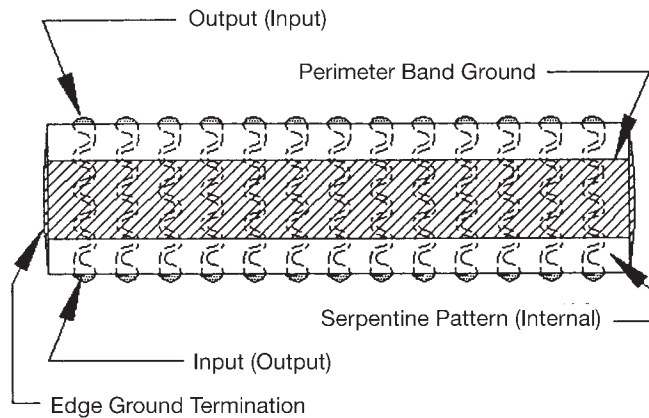


Figure 10. Serpentine Array

depicted in Figure 10 is used. This device contains 13 individual signal paths with the ground plane running

the full width of the array. Contact to each path is made at termination bands on opposite edges along the width of the array. The ground connection is made along the full face of the width and wrap over edge terminations along the lengths edge. The 13 paths were chosen to allow for a 25 pin D-Sub connector where one array is used for the top row of 13 pins and the second array is used for the bottom row of 12 pins (one capacitor is wasted to eliminate multiple requirements within one connector).

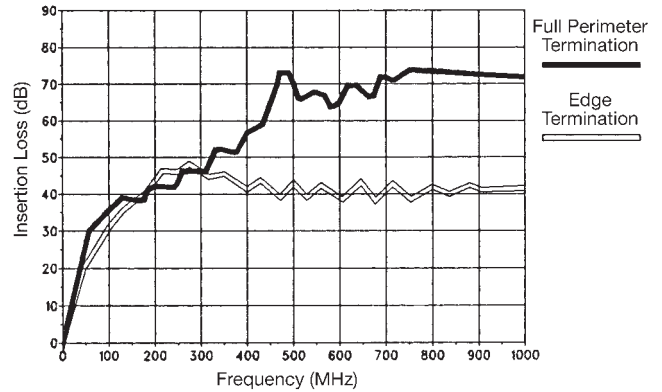


Figure 11. Insertion Loss Serpentine Feedthru (6 nFd) 13 Pin Array/Center Pin Measured

The full face termination is required to reduce the unequal inductive paths found in the ground plate, with the center paths as compared to the outside paths. This fix actually presents another small capacitance in parallel with the internal capacitance (almost as the internal is made up of the sum of all internal layers). The difference between the internal capacitance (full perimeter) and this small shunt capacitor is seen in the high frequency response of Figure 11.

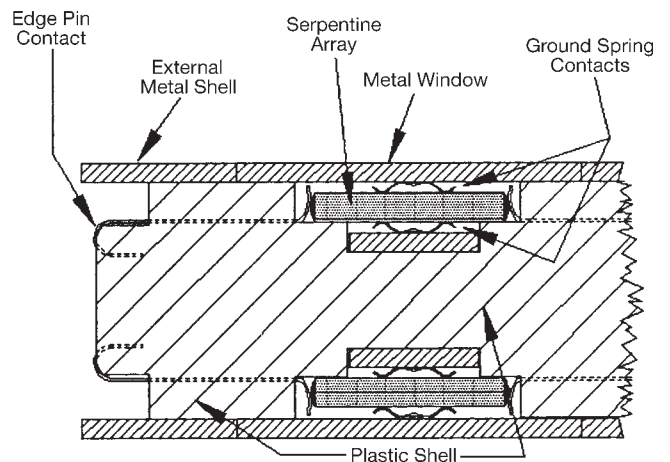


Figure 12. Serpentine Array Connector Shell



There is very little inductance associated with the full face termination because of the multiple contacts between it and the shell as shown in Figure 12. As the inductance of the internal ground circuit causes the internal capacitance to reach self-resonance, it is paralleled with this external plate capacitance. Its reactance continues to decrease with frequency, negating the rising impedance due to the now inductive internal element. Again, Figure 11 shows the effects of this full face termination.

## Serpentine Filter Connectors

These devices can be pressure/contact fitted into a shell. Spring force used to make the signal connection as well as ground connections as in Figure 12. They may also be soldered following the care required of any large MLC device.

The pressure contact is easily assembled and if ever necessary, easily repaired. This device lends itself to the rectangular connectors, yet may be used in a circular if pins can be divided into rows.

## Surface Mount Capability

These devices are fairly large for ceramic capacitors, ranging in size from the 2225 chip to 1 inch square. As such, we recommend *against* mounting these devices directly to the circuit board. For the *PEO* series, these devices are offered with a DIP type leadframe as a standard offering. They may also be built using a ribbon lead material. The large face termination of the *PE Power Plane Decoupling* capacitor must be connected to the circuit board by means of ribbon or multiple tabs bonded to it and the board, to allow independent coefficients of expansion to take place (between the ceramic component and the board).

The leads or leadframes are attached with a high temperature solder (9.0% Sn / 89.5% Pb / 1.5% Ag - 268°C to 290°C ). There will be approximately a 25 mil elevation from the device to the board. A slight angle of bend will add to the flexural capabilities of the contact.

Recommended solder profiles for all devices are available upon request. These devices are ceramic, and as such cannot be hammered or subjected to rough handling without damaging the unit. The device will survive all the environmental stress experienced in military specified testing if it is mounted with care. Unless all precautions are followed, mounting can damage the part to cause immediate or subsequent failure.

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