

TECHNICAL PAPER

Improved Noise Suppression Via MLCCs in Power-Entry Decoupling

Arch G. Martin

KYOCERA AVX Components Corporation
Myrtle Beach, S.C.

R. Kenneth Keenan

TKC
Pinellas Park, FL

Abstract

A new decoupling technique is proposed for surface mounted designs that recommends using 0.1 μF MLCs as the circuit-level decoupling capacitors and 1.0 μF to 10 μF MLCs in place of the tantalum as the board-level power-entry capacitor. This combination of MLCs on each PCB coupled with a single system level tantalum or aluminum is probably an optimum arrangement; performance is enhanced, and cost is not increased.

IMPROVED NOISE SUPPRESSION VIA MULTILAYER CERAMIC CAPACITORS (MLCs) IN POWER-ENTRY DECOUPLING

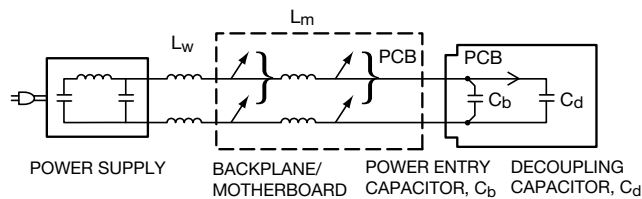
Arch G. Martin and R. Kenneth Keenan

Introduction

In a typical power distribution system (Figure 1-a), the power-entry capacitor C_b , is a relatively large-valued capacitor near the power-entry point on the PCB. The purposes of power-supply decoupling shown in Figure 1-b are to:

- Prevent transmission of PCB-generated noise to the backplane/motherboard and power supply.
- Supply charge to the power entry capacitor so that the voltage at the PCB power entry point is maintained at V_{cc} (usually 5 VDC).
- Suppress power supply backplane ringing resulting from inductance of power supply (L_w) and backplane (L_m).

In the past, these board level decoupling applications or power-entry capacitors have been dominated by aluminum electrolytic and tantalum capacitors, but the push into surface mount configurations presents major problems in the use of these electrolytic capacitors. Exposure of aluminum to Floroinert vapors used in vapor phase soldering (VPS) is detrimental to aluminum. In addition, aluminum electrolyte boils at VPS temperatures and also at IR (infrared) reflow temperatures (207-215 degrees C). Solid tantalum capacitors on the other hand have radically different coefficients of expansion between the tantalum slug, lead frame and epoxy resin body. This, coupled with the non-metallurgical bond of the cathode electrode, limits tantalum capacitor soldering temperatures to well below the normal temperatures used in surface mount assembly. Both aluminum and tantalum electrolytic capacitors must receive special handling at lower temperatures than the rest of the surface mount assembly for optimum electrolytic capacitor reliability.



1a. Power supply to printed circuit board (PCB)

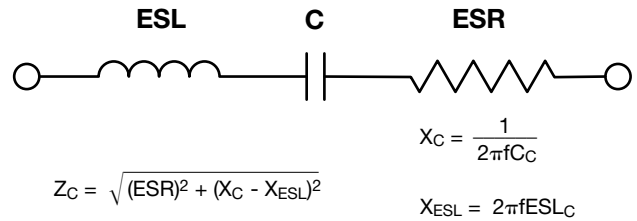
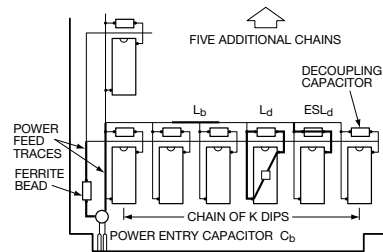


Figure 2. Total capacitor impedance

These factors, coupled with higher speeds, greater density, the need for improved emissions performance, increased reliability, and the trend toward distributed power supplies, have all served to focus upon the need for better and more efficient decoupling techniques, including capacitive decoupling at the power entry point, C_b .

Recent advances in ceramic technology have increased MLC volumetric and cost efficiencies such that high value, small physical size capacitors are now practical and able to compete with electrolytics. MLCs are compatible with surface mount processing and do not have the limitations of electrolytic capacitors. In addition, they are non-polar, which eliminates a major source of surface mount assembly defects stemming from polarity of electrolytics during assembly.

Power-entry filtering performance of MLCs is far superior to that of electrolytic capacitors, as MLCs are characterized by much lower values of ESL and ESR. These characteristics, plus newer high capacitance values, make MLCs ideal power-entry capacitors.



1b. Printed circuit board (PCB)

Figure 1: Power distribution system for typical digital equipment

Additionally, some of the power-entry capacitance is shifted to a single system tantalum (see systems considerations below for suppression of backplane ringing).

This new approach requires revision of conventional decoupling thinking, but results in significant improvement in design, emissions, and reliability.

Conventional Approach

The conventional approach to PCB-level decoupling is to choose one decoupling capacitor per semiconductor package and one power-entry capacitor per PCB. Except on extremely large PCBs, capacitors at points intermediate to the power entry and decoupling capacitors are not required or recommended (References 1 and 2).

One aim of the conventional approach has been to minimize the value of the circuit level (C_d) decoupling capacitors. A lower bound on decoupling capacitance is set by charge drawdown (droop) considerations (Reference 1):

$$C_d \geq 9 \times \text{Sum of switched capacitance,}$$

where the switched capacitance is the sum of the output gate plus load capacitance associated with the semiconductor package. Typically, only half the output gates in a given semiconductor package (NAND, NOR, etc.) are being switched at a clock pulse transition; then, the switched capacitance is only one-half that of the total gate plus load capacitance. For the layout of Figure 1b with 5 output gates per DIP being switched and with each output gate fanned out to two input gates, the assumption of LSTTL technology ($C_{out} = 20$ pf, $c_{in} = 5$ pf) leads to:

$$C_d \geq 9 \times 5 \times (20 + (2 \times 5)) = 1,350 \text{ pf} = 0.00135 \mu\text{F},$$

(Next highest standard value = .01 μF)

The value of the power entry capacitor is chosen large enough to handle the relatively low-frequency task of recharging the decoupling capacitors between each transition of the clock pulse:

$$C_b \geq 10 \times \text{Sum of decoupling capacitors } (C_d) \text{ on PCB.}$$

Care is taken not to use an overly-large power-entry capacitor, which is likely to exhibit excessive ESL and result in undesirable emissions.

For the example in Figure 1b with six six-DIP chains:

$$C_b \geq 10 \times 36 \times 0.01 \mu\text{F} = 3.6 \mu\text{F},$$

(Next highest standard value = 4.7 μF)

A ferrite bead is used at the power entry point to prevent low-frequency ringing and to minimize troublesome high-frequency clock-harmonic voltage at the power entry point. The relatively high-speed gate currents required *during* a clock transition are largely supplied by the decoupling capacitors, C_d , located close to the gates to which the current is supplied.

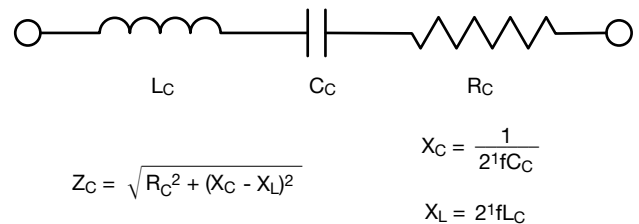


Figure 2: Total capacitor impedance

Ideally, the equivalent series inductances (ESLs) and resistance (ESRs) of both the power entry and decoupling capacitors (Figure 2) would be zero, as the impedances of those capacitors would be minimum. This provides maximum reduction in the transfer of switched-gate noise back to the power-entry point. Excess ESL, together with excess trace inductance and/or trying to load a single decoupler with too many semi-conductor packages, causes high-frequency ringing. Those clock-harmonic currents which are nearest the ringing frequency are transmitted to the power bus with little attenuation, causing emissions problems.

New Decoupling Techniques

The conventional approach has been to choose the decoupling capacitor as the lowest standard value in order to minimize both ESL, ESR, and cost. Improvements in multilayer ceramic capacitor (MLC) technology over the past few years has greatly changed designers' dependency upon these factors.

With improved MLC technology has also come reduced cost for higher values (Figure 3). Today, MLCs are less dependent upon high-cost metals due to less expensive electrodes materials.

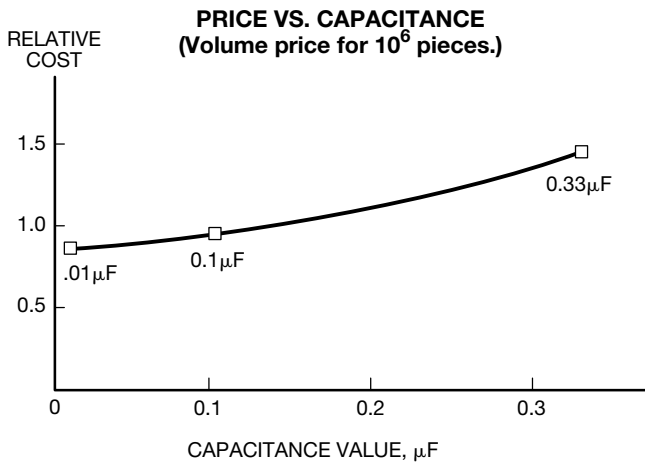


Figure 3: Cost of MLCs (volume purchased = 1,000,000 pieces)

The smaller size of today's MLCs has greatly reduced inductance variation with increasing capacitance value. The effective inductance can be measured via MLC response to pulse-edge rate of 200 ma/10 ns. Figure 4 shows that there is less than 1 nH difference between a 0.068 μF and a 1.0 μF. This low inductance for higher values allows the capacitance value to be chosen by the current requirements, not the capacitor's inductance. This frees the designer to increase the value of the decoupling capacitors and decrease the required value of the power entry capacitor to gain the advantage of the lower ESLs and ESRs associated with power-entry MLCs.

The inductance of the wires/traces between the power supply and the power entry capacitors suggest that, for worst-case low-frequency charge

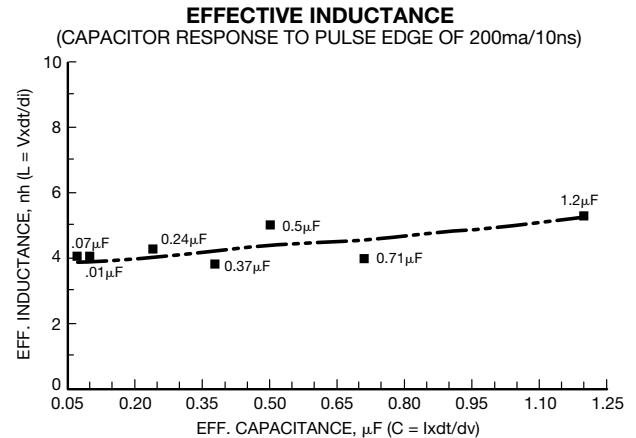


Figure 4: Effective inductance (ESL) of AVX MLC dipped radials (Lead length ≈ 0.100")

replenishment purposes, the decoupling capacitors are in series with the power-entry capacitor (no reliance on the power supply between clock pulses). In terms of the preceding example: If we decrease the size of the 4.7 μF power entry capacitor to 1.0 μF (MLC), how much would the values of the decouplers have to be increased in order to maintain an effective total decoupling capacitance of 0.01 μF/DIP x 36 DIPs = 0.36 μF?

$$\frac{(Total C_d)(1.0)}{1.0 + (Total C_d)} = 0.36, Total C_d = 0.563 \mu F$$

If decouplers had been chosen at the 0.00135 μF lower limit, they would have to be increased to 0.563/36 = 0.0156 μF. In practice, a decoupling value of 0.1 μF can and is generally used anyway.

This design approach allows the power entry capacitor value to be reduced to take advantage of the lower ESL and ESR of MLC capacitors. This will result in maximum reduction of transmitted switched-gate noise back to the power-entry point and the back panel of the total system. As shown in Figure 5, this reduction is, relative to that provided by the conventional approach (4.7 μF power-entry capacitor), greater than 15 dB in the critical range of clock-harmonics falling between 50 MHz and 150 MHz. This is the most troublesome frequency range in meeting FCC emission requirements, as that noise will eventually find its way to an "antenna" (I/O cables, etc.) and cause out-of-spec emissions problems.

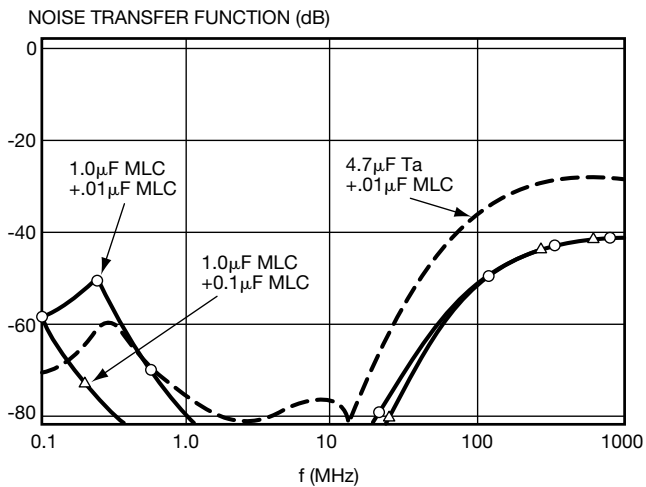


Figure 5: Noise transfer function from switched gates to power entry point

System Level Considerations

In the conventional approach, the aggregate of all power-entry capacitors is used to suppress power supply backplane ringing which would otherwise arise due to the inductance of the power supply (L_w) and backplane/motherboard (L_m):

Backplane Capacitance =
Sum of Power Entry Capacitance (all PCBs)

$$\sum C_d \geq \frac{4(L_w + L_m)}{R^2}$$

where R is the effective resistance of the power supply. For 250 nH of $L_w + L_m$ and an effective R of 0.1 Ohm, the sum of the power entry capacitors on the PCBs distributed along the backplane must exceed 100 μ F. Instead of multiple high-value power-entry capacitors, this total backplane capacitance requirement can be met by using a single tantalum capacitor at the point where the power supply wires connect to the backplane or motherboard. Then, smaller-valued power-entry MLCs can be used on each PCB, resulting in the aforementioned high-frequency emissions and reliability improvements.

In small systems using local area power supplies, the addition of the tantalum capacitor for backplane capacitance would normally not be necessary.

Conclusions

A new decoupling technique is proposed that recommends using 0.1 μ F MLCs as the circuit-level decoupling capacitors and 1.0 μ F to 10 μ F MLCs in place of the tantalum as the board-level power-entry capacitor. In addition, a system-level electrolytic may be required in the power supply distribution decoupling network.

The above combination of MLCs and PCBs coupled with a single tantalum is probably an optimum arrangement; performance is enhanced, and cost is not increased. If anything, it is decreased due to the increased reliability of MLCs relative to surface mounting, and where the cost of tantalum chips are high and require special handling and design considerations.

References

- (1) R.K. Keenan, Decoupling and Layout of Digital Printed Circuits, Pinellas Park, Florida: TKC, 1985.
- (2) A. Martin and W. Parkinson, "Functional Testing of Decoupling Capacitors for Dynamic RAMs", AVX Application Note, 1983.



NORTH AMERICA
Tel: +1 864-967-2150

ASIA
Tel: +65 6286-7555

CENTRAL AMERICA
Tel: +55 11-46881960

EUROPE
Tel: +44 1276-697000

JAPAN
Tel: +81 740-321250

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