TECHNICAL DOCUMENT

Selecting KYOCERA AVX RF Chip Capacitors for Wireless Applications

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INTRODUCTION

With today's advancements in wireless technology, greater emphasis is being placed on component performance. This article will provide a discussion of ceramic and porcelain chip capacitors and understanding their behavior in RF product designs. They are an excellent choice for wireless applications where volumetric efficiency, reliability and RF performance are an absolute must.

DESIGN CRITERIA

The most commonly used design categories for KYOCERA AVX ceramic chip capacitors are the multilayer (MLC) and single layer (SLC). The MLC employs multiple or stacked electrode sections while the SLC consists of two electrodes separated by a dielectric. Both are constructed with the following design criteria:

- Ceramic and porcelain dielectrics
- Rugged hermetic construction
- Optimized electrode patterns
- Low resistivity electrode and termination materials
- High dielectric strength
- Protective barrier layer between electrodes and termination (MLC)
- Fabricated for direct surface mounting on microstrip
- Ultra stable with temperature and humidity
- Extremely high Q
- Low dissipative losses

SELECTING A SUITABLE CAPACITOR

When selecting ceramic chip capacitors for use in RF wireless applications, it is important to establish overall circuit performance criteria. The component should then be matched to the specific application requirement. A typical shopping list of performance requirements for this circuit element may include the following:

- Ceramic and porcelain dielectrics
- Rugged hermetic construction
- Optimized electrode patterns
- Low resistivity electrode and termination materials
- High dielectric strength
- Protective barrier layer between electrodes and termination (MLC)
- Fabricated for direct surface mounting on microstrip
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- Low dissipative losses

PERFORMANCE

An ideal capacitor stores all of its energy in the dielectric, as $1/2CV^2$. However, a realizable capacitor will always exhibit some series resistance that must be taken into account. This series resistance referred to as Equivalent Series Resistance (ESR) is always one of the most essential factors to consider in an RF circuit design. It is attributed mainly to the contribution of dielectric losses, and metal losses of electrode and termination materials. Also, the manufacturing process must be properly controlled during every phase to insure optimal ESR performance. At low frequencies, Hz to KHz region, the main contributor to ESR is dielectric loss. However, at RF frequencies the ESR is due mainly to the metal losses, i.e., electrodes and terminations. These losses become significant because of skin effect and increase proportionally as the square root of frequency.

ESR is typically expressed in milliohms at specific frequencies by most manufacturers. The standards most frequently used as a guideline are EIA RS483 and MIL-C-55681. The measurements are performed at various frequencies between 30 MHz and 1 GHz. Therefore, it is necessary to consider the ESR value at your specific design frequency. If, for example, you are designing for a 900 MHz wireless application, and the ESR is specified at 150 MHz, the ESR at 900 MHz may be calculated by multiplying the specified ESR at 150 MHz by √900/150. This relationship is well behaved at RF and accounts for the "skin effect". The ESR is the main loss element of the capacitor and is used to determine the power loss i.e.; $P = I^2 * ESR$.

Quality Factor (Q) is a figure of merit and is a measure of a capacitor's ability to store energy in its dielectric. Since Q = Xc/ESR, it becomes evident that low ESR yields high Q. As with ESR, the Q must be specified or calculated at the design frequency.

Dissipation Factor (DF) is also referred to as the loss tangent and is the reciprocal of Q, i.e., DF = 1/Q. With an ideal capacitor the current leads the voltage by 90 degrees. However, actual capacitors will have a small angle referred to as the loss angle. The tangent of the loss angle is equal to the dissipation factor and indicates what portion of the total reactive power in the capacitor will be lost as heat i.e., dissipative loss.

Example:

Loss angle = 3 degrees;
therefore DF = tan 3 = 0.05 or 5%

In the above example, the dissipation factor is 0.05 or 5%. This means that 5% of the total power in the capacitor is lost as heat. Refer to **Figure 1**.

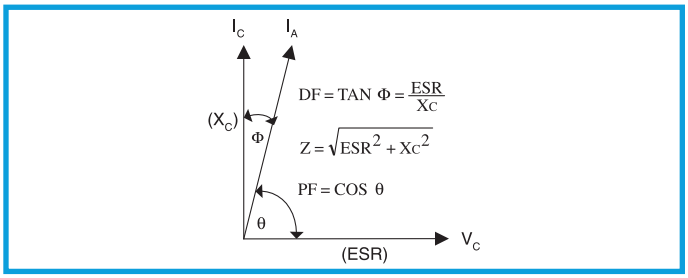

Figure 1. Dissipation Factor

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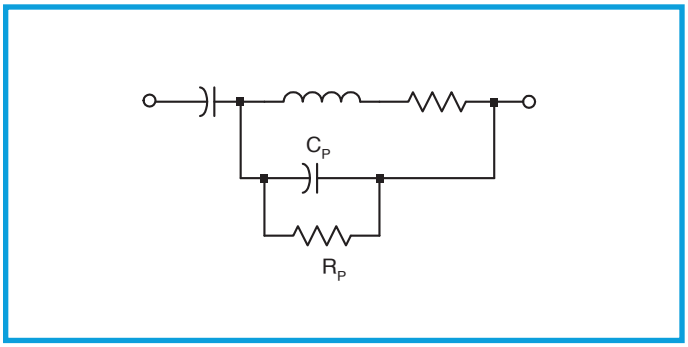

Figure 2. Equivalent Circuit Model

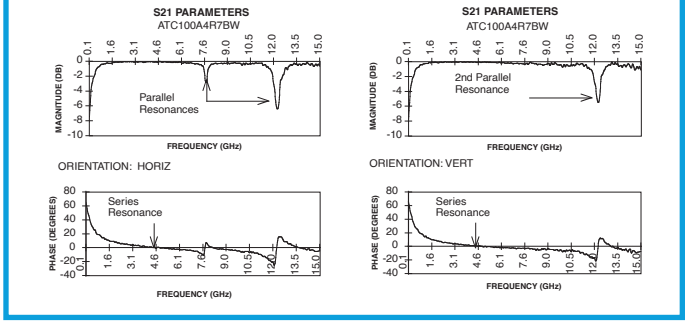

Figure 3. S-Parameter Plots comparing horizontal and vertical mounting orientations

The KYOCERA AVX 100 Series porcelain chip capacitors have a loss tangent less than 0.0001 that yields a Q greater than 10,000. In this instance the dissipative losses are less than 0.01%. This is desirable for optimum performance in an RF circuit. An amplifier circuit for example, that utilizes a high Q, low ESR (DF) capacitor will realize a significant increase in the effective gain. Battery life for portable devices is also extended with the use of low loss capacitors. An easy way to relate ESR, DF, a Q together is:

ESR, DF and Q together is:
ESR = Xc DF =Xc/Q
DF = ESR/Xc

PARASITIC BEHAVIOR

Another major concern in wireless design applications is the parasitic behavior of the reactive elements. Capacitors may be modeled with equivalent circuit elements that account for the parasitic effects. **Figure 2** shows a lumped element model and is valid for chip capacitors in these applications. Using this model can help the designer determine such characteristics as the series resonant frequency (Fsr), equivalent series inductance (ESL) and transfer function characteristics.

It is necessary to consider the functional application, e.g., coupling, bypass, timing etc., and layout in the circuit. For example, a given application may require a capacitor for interstage coupling. A more thorough view of parasitic behavior is accomplished by the use of scattering parameters. KYOCERA AVX specifies S-Parameter performance for their capacitor line.

In the above example it is important to evaluate the S-Parameter performance for the subject capacitor. If a parallel resonance occurs at or near the frequency band of interest, this capacitor will serve to attenuate the RF energy rather than it's intended coupling function. S-Parameter data will show such characteristics as parallel resonance, series resonance, insertion loss, insertion phase, return loss magnitude and return loss phase.

A full set of S-Parameters may be used in conjunction with design simulation software, and is generally presented as a forward and reverse two port measurement known as an S2P file.

COMPONENT ORIENTATION

Chip capacitors are usually surface mounted on a microstrip. They can be mounted with the electrodes parallel or perpendicular to this microstrip. In the above example a coupling capacitor is used between stages. As previously mentioned it is essential that parallel resonances do not occur in the frequency band of interest. By mounting the capacitor vertically, that is, with the electrodes perpendicular to the microstrip, the first parallel resonance will not be present thereby significantly extending the usable bandpass. A comparison of the two mounting orientations using S-Parameters is shown in **Figure 3**.

Series Resonant Frequency:
Occurs at the frequency corresponding to 0 degrees phase of S21; also S21 magnitude has minimum loss at this frequency equal to ESR.

Parallel Resonant Frequencies:
Are observed as a sharp attenuation in the S21 magnitude while S21 phase has rapid transitions through 0 degrees corresponding to each parallel resonance. Vertical mounting optimizes this performance.

S21 Magnitude 3DB Frequency:
Capacitance value may be verified at this frequency by C = 0.159/100*F (Hz).

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