TECHNICAL PAPER

Very High Frequency Switch Mode Power Supply Output Filter Capacitor Considerations and Mounting Limitations

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Abstract:

This paper discusses output filter capacitor electrical limitations and considerations when used in 1MHz and above switch mode power supplies. Because surface mount components and assembly will be used to build these very high frequency switchers, physical mounting limitations, mechanical stress and assembly techniques are also discussed.

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VERY HIGH FREQUENCY SWITCH MODE POWER SUPPLY OUTPUT FILTER CAPACITOR CONSIDERATIONS AND MOUNTING LIMITATIONS

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The drive for greatly increased power densities in switch mode power supplies (SMPS) is dramatically pushing the switching frequency up as a method for increased power density. This increase in switching frequency now puts severe limitations on the output filter capacitor's electrical parameters and how it is physically mounted in the circuit.

Historically, ESR (equivalent series resistance) has been the primary output filter capacitor parameter that dominated output ripple voltage. The amount of capacitance required to meet this ESR requirement has been 10 - 1000 times the minimum capacitance that is needed for the power supply and the large number of capacitors used to get low ESR significantly reduced the effective ESL (equivalent series inductance). This has changed with switching frequencies departing from the 200 KHz range and moving into the 1 MHz and beyond. ESR is no longer the single dominant factor in output filter ripple and noise voltage, now ESL also becomes a limiting parameter for output filter capacitors.

Total output filter inductance should be 1 nH or less for many high frequency SMPS designs. This forces designers to consider surface mount (SM) components to eliminate inductance. Traditional output filter technologies must be abandoned in

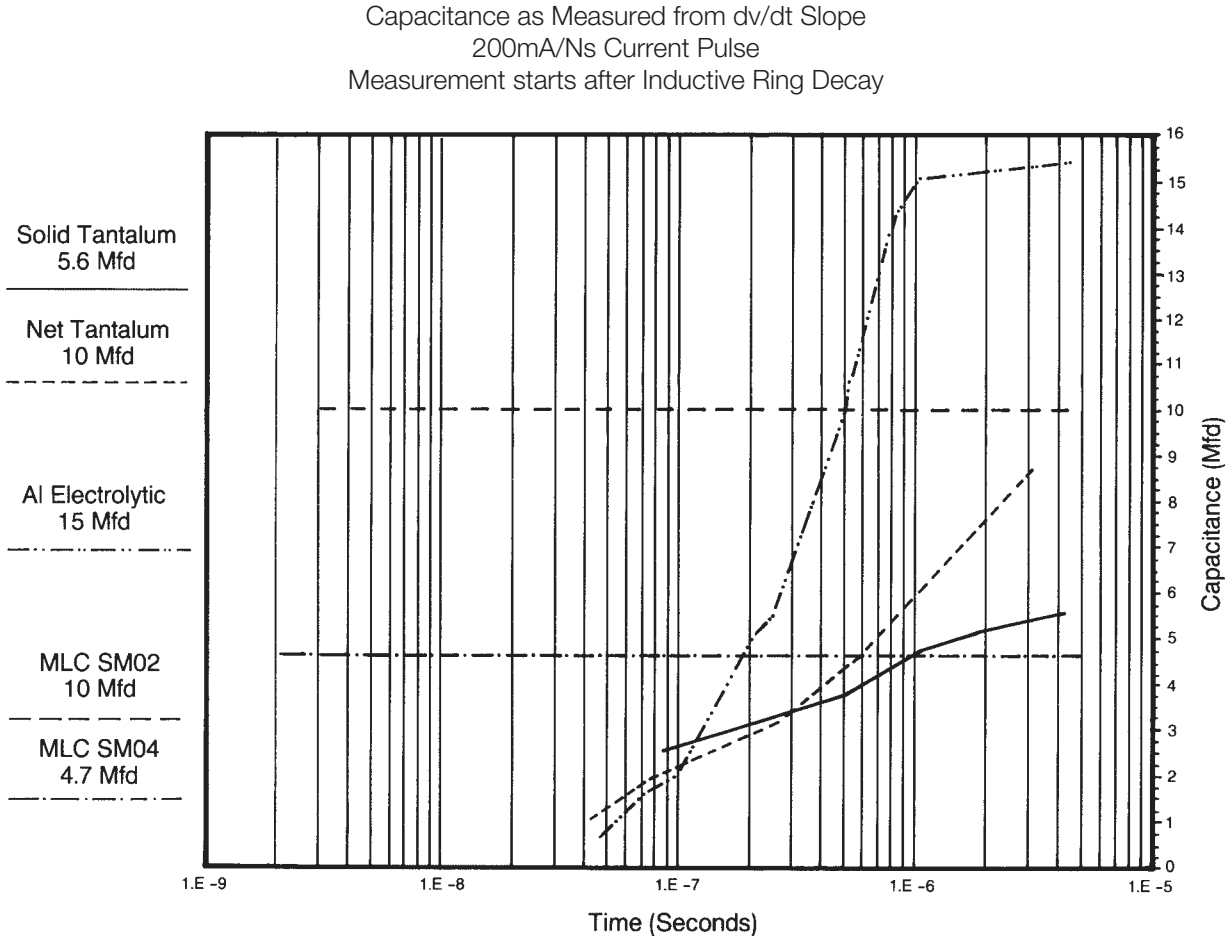

Figure 1. Effective Capacitance vs Time for Ceramic MLC, Electrolytic and Tantalum Capacitors

favor of new capacitors with configurations and characteristics that will meet these future needs. Electrolytic capacitors are just not suitable for these applications because of high ESR and ESL. In addition they require special handling for surface mounting because the electrolyte boils at the reflow soldering temperatures and aluminum reacts violently with vapor phase soldering fluids. Tantalum capacitors have very high values of ESR and are difficult to surface mount reliably. SM tantalum capacitors have a failure mode that is accelerated by reflow soldering and causes ESR to increase with time.

Tantalum and aluminum electrolytic capacitors' intrinsically high ESR and ESL dramatically reduce their usable capacitance at high frequency as shown in Figure 1. Since film capacitors polymers melt at solder reflow temperatures, this leaves multilayer ceramic (MLC) capacitors as the only viable alternative for very high frequency SMPS output filters..

Traditional MLC capacitors are not designed for absolute minimum ESL and ESR but instead are designed to meet the competitive commercial and military market place for integrated circuit decoupling. Capacitors that are to be used as output filters in high frequency/high power SMPS need to be designed to minimize these parameters in order to maximize ripple current capability.

Guidelines need to be established for practical output filter capacitor limits of minimum required capacitance and maximum ESR and ESL. Most switch mode power supplies have high ripple currents similar to Figure 2. This ripple current is for a simple L-C output filter and is typical of a forward or flyback converter. Different designs will have different but similar current waveforms and filter requirements.

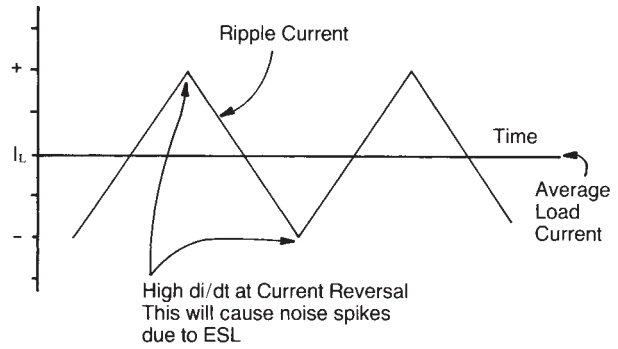

Figure 2. Output Filter Capacitor Current 1c

This ripple current will cause a ripple and noise voltage that is due to the capacitor's value, ESR and ESL. The high voltage swings are due to ESL in high frequency switchers because of high di/dt at the current inflection points. Increases in frequency or ripple (load) current proportionally increases di/dt and thus noise. Remember V = L di/dt where L is the output filter capacitor's inductance, di/dt is the rate of change of current with respect to time and V is the voltage spike amplitude. An order of magnitude increase in operating frequency or load current decreases the maximum allowable ESL by the same amount. As frequencies and load currents continue to increase for improved power densities, the output filter capacitor must be incorporated into a transmission line structure to cancel its inductance. The current drive to take switching frequencies beyond 10 MHz will force the output filter into cavities and new configurations to further reduce filter inductance.

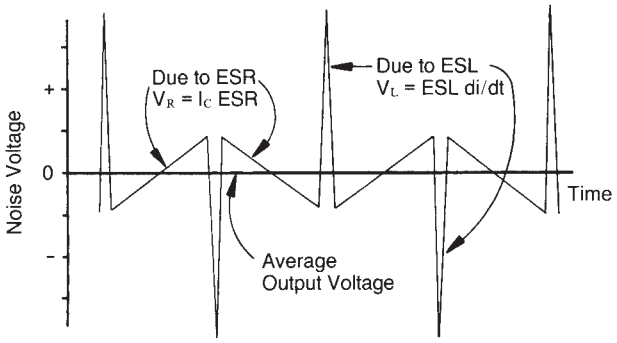

Figure 3. Output Filter Noise due to ESR and ESL

When the current waveform in Figure 2 is analyzed, practical limits for ESR_{max}, ESL_{max} and minimum output filter capacitance (C_{min}) can be established. Each limit is derived assuming that there is no contribution to output ripple and noise from the other two parameters. For example the values of C_{min} are calculated assuming that all ripple is from the capacitance. In practice more capacitance is used to minimize its contribution to output ripple and in some cases much more is needed to stabilize the power supply control loop. When that is the case, a lower value high performance output filter capacitor should be used in parallel with a higher value capacitor to provide loop stability. Figures 4, 5 and 6 show these limits for C_{min}, ESR_{max} and ESL_{max}.

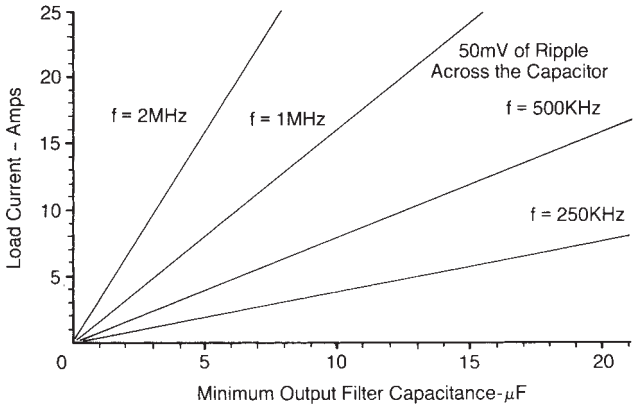

Figure 4. Minimum Output Filter Capacitance vs Load Current for an Inductor/Capacitor (L-C) Output Filter

The above plot assumes that there is no capacitor ESR or ESL and is used to set a minimum required capacitance for the output filter. Typically two to three times this capacitance is a more real number due to ESR and ESL limitations. It is much higher when tantalum or electrolytic output capacitors are used. The following equation was used to generate these curves.

$C_{min} = \Delta I_{out}/8f\Delta V_{out}$

With $\Delta I_{out} = 0.25I_{out}$, I_{out} = Load Current

ΔV_{out} = Maximum Output Ripple Voltage

f = Switching Frequency

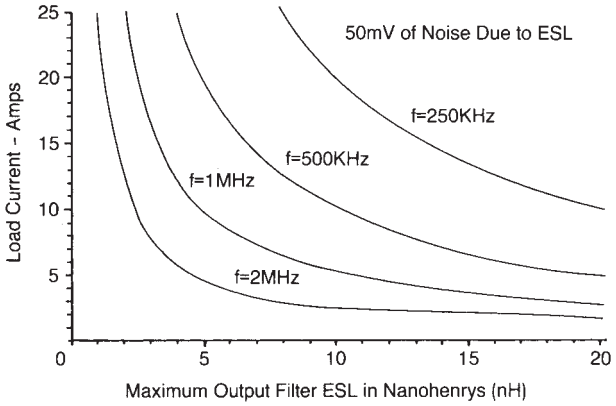

Figure 5. Maximum Output Filter ESL in nH for 50 mV of Noise vs Output Load Current

The above plot assumes that there is no ripple voltage due to the capacitor (infinite capacitance) and ESR is zero. Typically, one-half to one-third of the total ripple and noise voltage is due to ESL so divide the numbers from the graph by two or three to get a real ESL value. The following equation was used to generate these curves.

$ESL_{max} = 0.25\ \Delta V_{out}/\Delta I_{out}f = \Delta V_{out}/I_{out}f$

With ΔV_{out} = Maximum Noise Voltage

ΔI_{out} = Ripple Current

or $\Delta I_{out} = 0.25I_{out}$, Load Current

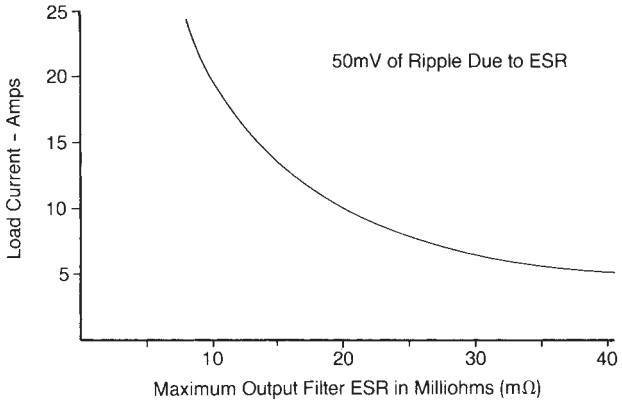

Figure 6. Maximum Output Filter ESR in mΩ for 50 mV of Ripple vs Output Load Current

The above plot assumes that there is no ripple voltage due to the capacitor (infinite capacitance) and ESL is zero. Typically, one-third to one-fourth of the ripple and noise voltage in high frequency switch mode power supplies is due to ESR so divide the numbers from the graph by three or four to get a real ESR value. The following equation was used to generate this curve.

$ESR_{max} = \Delta V_{out}/\Delta I_{out} = 4\Delta V_{out}/I_{out}$

With ΔV_{out} = Maximum Ripple Voltage

ΔI_{out} = Ripple Current

or $\Delta I_{out} = 0.25I_{out}$, Load Current

With maximum total inductance values in the range of 1-2 nH total for the output filter, surface mount components and RF layout techniques are mandatory for very high frequency SMPS that operate at 1 MHz and above. Unfortunately, we just can't slap a few capacitors on a substrate along with transistors, diodes, resistors and inductors that has ground plane everywhere and expect it will work reliably. There are practical size limitations for MLCs that prohibit reliable direct mounting of chip capacitors larger than 2225 (.22" x .25") to a substrate. These large chips are subject to thermal shock cracking and thermal cycling solder joint fatigue. Even 1812 (.18" x .12") and 2225 chip capacitors will have solder joint failures due to mechanical fatigue after ≈ 1500 thermal cycles from 0 to 85°C on FR4 and ≈ 3000 cycles on alumina from -55 to 125°C. This is due differences in the Coefficient of Thermal Expansion (CTE) between MLCs and substrate materials used in hybrids and surface mount assemblies. Materials used in the manufacture of all electronic components and substrates have wide ranges of CTEs as shown in Table 1.

MATERIAL	CTE (ppm/°C)
Alloy 42	5.3
Alumina	≈7
Barium Titanate Capacitor Body	9.5-11.5
Copper	17.6
Copper Clad Invar	6-7
Filled Epoxy Resin ($<T_g$)	18-25
FR4/G-10 PC Board (X, Y)	≈18
Nickel or Steel	15
Polyimide/Glass PCB (X, Y)	≈12
Polyimide/Kevlar PCB (X, Y)	≈7
Tantalum	6.5
Tin Lead Alloys	≈27

Table 1. CTEs of Typical Components and Substrates

This CTE difference translates into mechanical stress that is due to the linear displacement of substrate and component. Linear displacement is a function of ΔCTE (CTE_{sub} - CTE_{comp}) and the overall length of the component. Long components/ substrates have large linear displacements even with a small ΔCTE which will cause high stress in the solder joints and fatigue after a few temperature cycles. Figure 7 shows linear displacement for conditions where ΔCTE is positive and negative.

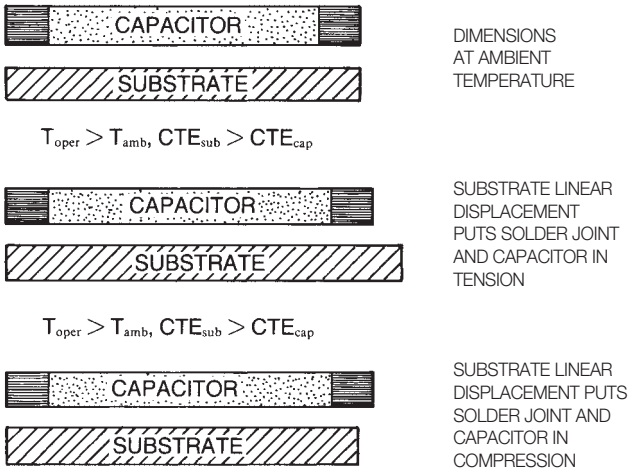

Figure 7. Linear Displacement Between Component and Substrate

Figures 8 and 9 show the location of maximum stress in the solder joint due to positive and negative ΔCTE and linear displacement.

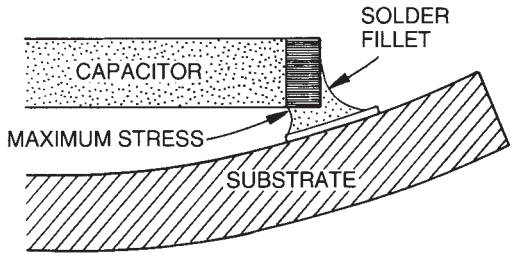

Figure 8. Stress for $T_{oper} > T_{amb}$ and $CTE_{sub} > CTE_{cap}$

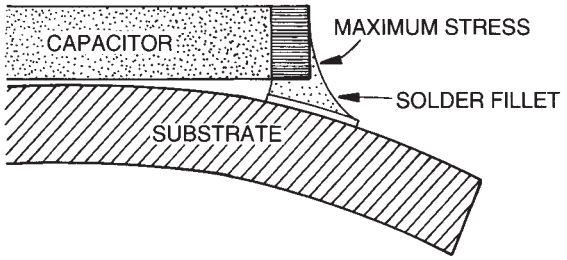

Figure 9. Stress for $T_{oper} > T_{amb}$ and $CTE_{sub} > CTE_{cap}$

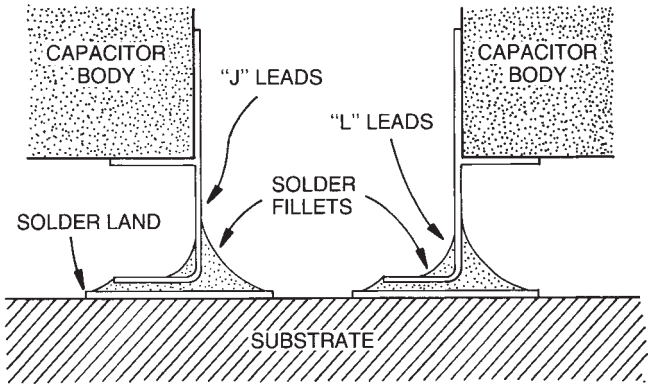

Figure 10. "J" and "L" Leadframes Mounted on Capacitors to Relieve Stress

Leadframes on larger capacitor sizes (greater than 2225) must be used to minimize mechanical stress on the solder joints during temperature cycling which is normal operation for power supplies. Failing solder joints increase both ESR and ESL causing an increase in ripple, noise and heat, accelerating failure.

Effective solder dams must be used to keep all molten solder on the solder lands during reflow or solder will migrate away from the land, causing opens or weak solder joints. High frequency output filters cannot use low power layout techniques such as necked down conductors because of the stringent inductance requirements.

Adding leadframes has a small impact on component inductance but this is the price that must be paid for reliable operation over temperature. Figure 11 shows typical leadframe inductance that is added for two lead standoff distances (0.020" and 0.050") versus the number of leads along one side of SupraCap™ which are specifically designed output filter capacitors for 1 MHz and above switchers. The actual inductance will be somewhat less because the leadframes flare out from the lead where the leadframe is attached to the capacitor body.

Very high frequency switch mode power supplies place tremendous restrictions on output filter capacitors. In addition to handling high ripple current (low ESR), ESL must approach zero nano henrys, parts must be truly surface mountable and be available in new configurations to be integrated into transmission lines to further reduce inductance with load currents greater than 40A at 1 MHz and as frequencies move above 1-2 MHz.

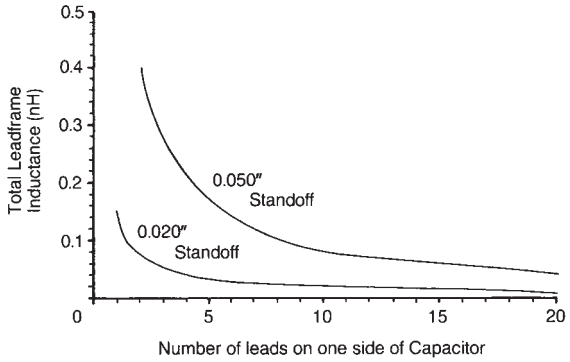

Figure 11. Number of Leads on One Side of Capacitor vs Total Leadframe Inductance vs Substrate Standoff Height

The total inductance is the sum of each side of the part where the inductance of one side is the parallel combination of each lead in the leadframe. That inductance is given by:

$L(nH) = 5xl[\ln(2xl/(B+C)+1/2]$

Where I = lead length in inches

In = natural log

B+C = lead cross section in inches

so $L_T(nH) = 2xL(nH)$ where L_T is the total inductance of the leadframe

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