

# TECHNICAL PAPER

## Processing Guidelines for S.M.P.S. Multilayer Ceramic Capacitors

**John Maxwell and Mark Doty**

*KYOCERA AVX Components Corporation*  
Olean, NY

---

### **Abstract:**

Surface mount technology and high current layout techniques will be used as high frequency switch mode power supplies move to one megahertz and beyond. There are practical SMT size limitations to components without compliant leads due to solder joint failure but adding leadframes to larger parts does not degrade electrical performance while enhancing reliability.



# PROCESSING GUIDELINES FOR S.M.P.S. MULTILAYER CERAMIC CAPACITORS

by John Maxwell and Mark Doty  
KYOCERA AVX Components Corporation  
Olean, NY

## Introduction

The drive for greatly increased power densities in switch mode power supplies (SMPS) has pushed switching frequencies to one megahertz and beyond. This switching increase now puts severe limitations on output filter capacitor electrical performance, capacitor technology, and mounting techniques. Traditional capacitor solutions no longer work at these higher frequencies because ESR (equivalent series resistance) is not the limiting electrical parameter; performance or ripple voltage is now limited by ESL (equivalent series inductance).

The amount of capacitance required for older low frequency switchers has been 10-1000 times the minimum capacitance required to achieve desired ESR values. Switching noise due to inductance in output networks is now limiting output ripple and not resistance. Output filter inductance values are now limited to only a few nanohenries or less forcing designers to consider surface mount technology (SMT) to eliminate leads and its associated inductance. Shifting to SMT will reduce output filter capacitance values to actual minimums for physical size and inductance reasons. Also, traditional output filter technologies must be abandoned in favor of new capacitors with configurations and electrical characteristics that meet those future needs.

Electrolytic capacitors are not suited for surface mount assembly because the electrolyte boils at reflow soldering temperatures. Both electrolytic and tantalum capacitors have high values of ESR and ESL, precluding their use in very high frequency switchers. Film capacitors have electrical characteristics making them suitable for some switcher applications but plastic temperature sensitivity to soldering and huge sizes for high values will minimize their use in SMT high frequency switchers. This leaves multilayer ceramic (MLC) capacitors as the only viable alternative for very high frequency SMPS output filters.

Traditional MLC capacitors are not designed for absolute minimum ESL and ESR but instead are designed to meet the competitive commercial and military market place for decoupling integrated circuits. Capacitors that are used as output filters in high frequency/ high power SMPS are specially designed for very low ESR, ESL, and very high ripple current.

The transition from thru-hole manufacturing to surface mount assembly has made one thing crystal clear: components and substrates are easily damaged by the solder and assembly process. The entire assembly is subjected to the solder process when SMT is used, exposing components and substrates to high temperatures

for long periods of time. Unfortunately some materials, in particular plastics used to manufacture PC boards and IC packages, are not well suited for high temperature processing. Experienced users are finding out the hard way that PC boards, plastic molded ICs or transistors, and even solder places stringent limitations on assembly processing. MLC capacitors also impose their own set of limitations for thermal processing and stress due to physical size.

## Material Limitations

Output filter inductance values of a few nanohenries or less mandate the use of SMT and RF layout techniques in switchers that operate at 1MHz and above. Unfortunately we can't slap a few capacitors, transistors, diodes, inductors, and resistors on a PC board covered with ground plane, solder them into place and expect the assembly to work reliably. There are practical size limitations in soldering rigid components directly to substrates. Residual stress in solder joints and stress due to differences in coefficients of thermal expansion (CTE) between components and substrates precludes the use of rigid components larger than a quarter inch square in SMT power supplies. The initial residual stress in a 1206 (.126" x .063") capacitor solder joints when mounted on an FR-4 PC board exceeds 350 psi. Room temperature tensile strength of Sn62 or Sn63 solders is only about 5,000 psi, restricting rigid component size. Fractures in fatigued solder joints occur in high stress zones and are due to differences in CTE, component length, and temperature excursions. Figure 1 shows typical solder joint stress zones for PLCC (plastic leaded chip carriers) IC and chip components. Other SMT components like transistors, diodes, resistors, inductors, and transformers all have similar solder joint stress zones.

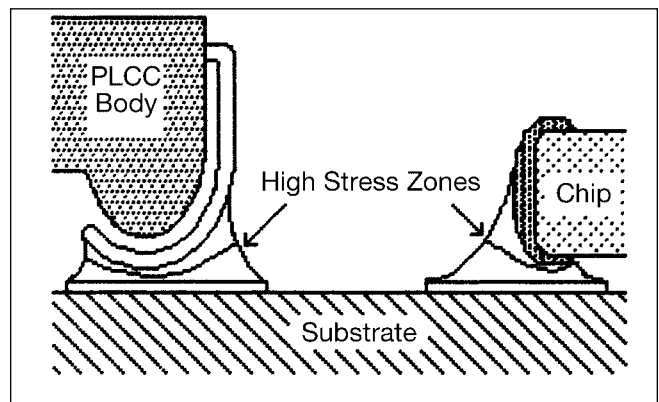


Figure 1. Solder Joint Stress Zones

Longer components have larger solder joint stress during temperature cycling due to large linear displacement which is the difference in length of a component and the substrate segment between solder pads during temperature excursions. Linear displacement is:

$$\Delta L = (L)(\Delta CTE)(\Delta T), \text{ where}$$

L is the initial segment length,  
 $\Delta CTE$  is the difference between component and substrate CTE, and  
 $\Delta T$  is the temperature excursion.

**Table 1. CTEs of Typical Components and Substrates**

Material	CTE (ppm/°C)
Ceramic Capacitor	9.5-11.5
Alumina	≈7
Copper	17.6
Copper Clad Invar	6-7
Filled Epoxy Resin (<Tg)	18-25
FR-4 PC Board (X<Y)	≈18
Nickel or Steel	≈15
Polyimide/Glass PCB	≈12
Polyimide/Kevlar PCB	≈7
Tantalum	6.5
Tin Lead Alloys	≈27

Figure 2 shows linear displacement for both PC boards where the CTE is greater than that of a component and a ceramic substrate where the opposite is true.

Stress is relieved in solder joints over time due to the ductile nature of solder but stress is created in solder joints during temperature cycling due to differences in CTE. Solder joint stress needs to be minimized due to temperature and CTE mismatch because of accelerated solder grain structure changes and reduced reliability.

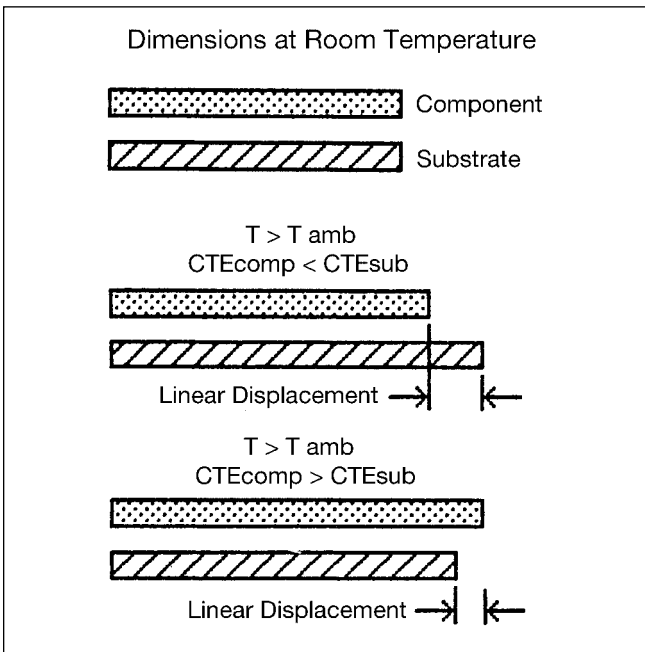


Figure 2. Linear Displacement for Different Substrate Conditions

Figure 3 shows the location of maximum stress in solder joints for different temperature and  $\Delta CTE$  conditions.

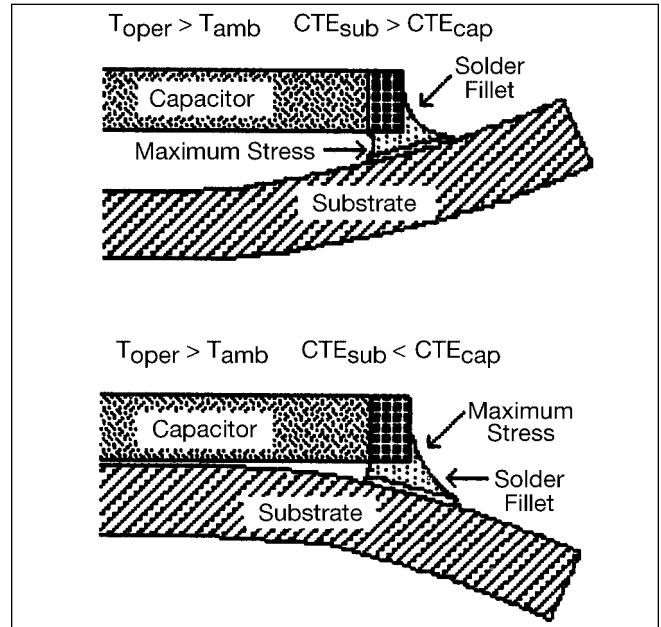


Figure 3. Solder Joint Stress for Different Temperature and  $\Delta CTE$  Conditions

Solder joint fatigue due to CTE differences mandates compliant leads on large components. Failing solder joints increase both ESR and ESL causing an increase in ripple, noise, and heat, accelerating system failure. Lead inductance must be minimized because of switching noise and ripple in the output filter but leads must be long enough to bend during temperature cycling in normal operation. The use of integrated circuit leadframes with 0.1" spacing meets both requirements, low inductance and bending during temperature excursions. Figure 4 shows total added leadframe inductance for between two and twenty leads with a 20 mil or 50 mil standoff between the component and substrate. These added inductance values do not degrade output filter noise while adding solder joint reliability.

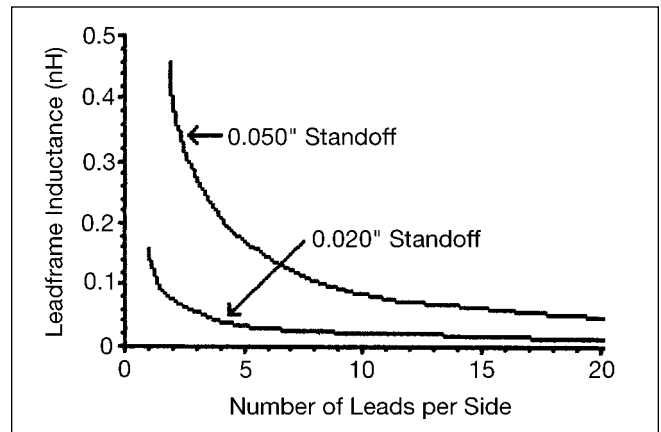


Figure 4. Inductance for Leadframe Lead Counts of 2-20 and Different Substrate/Component Standoff Heights

Total inductance is the sum of inductance on each side of the part which is the parallel combination of each lead in the leadframe. That inductance (1) is given by:

$$L \text{ (nH)} = 5 \times [\ln(2x1) / (B+C) + 1/2],$$

where

I = lead length in inches

In = natural log

B + C = lead cross section in inches

so LT (nH) = 2 x L (nH), where LT is the total leadframe inductance.

## Thermal Shock

Multilayer ceramic capacitors are complex mechanical structures (2) consisting of layers of barium titanate based ceramic, interleaved metal electrodes, and a metal termination. Rapid changes in temperature encountered during soldering results in mechanical stress (3) due to differences in CTE and temperature gradients within the device. An observed result is that large, thick parts are more sensitive to thermal shock than smaller parts, restricting solder processes. Typical SMT chip capacitors require preheat temperatures prior to soldering to be within 100°C to eliminate thermal shock cracks, but large MLCs used for SMPS output filters require much smaller temperature differences. Differences of 50°C or less are required for the largest MLC to eliminate thermal shock, precluding the use of direct component wave soldering as a process. This is not a real limitation because large components are not normally soldered to a board bottom without being washed off in the solder wave.

Thermal shock cracks in MLC capacitors may lead to excessive leakage currents and then component failure. Care must be taken during the assembly process to insure that there are no thermal shock cracks in any component. There are four common soldering processes used to manufacture power supplies: hand, wave or drag, infrared (IR) reflow, and vapor phase reflow soldering. Each assembly soldering technique has different limitations imposed due to thermal shock of components, excessive component heating, and degraded solder joints. Each soldering technique will be discussed and component/material limitations listed.

Mass solder processes need to be monitored and controlled to eliminate any damage to components or substrates. Process temperature profiles need to be run every shift with multiple thermocouples attached to various points on the assembly. Reflow soldering has the highest number of measurement points because components and substrate points need monitoring to insure no damage occurs. Proper profiling techniques are covered in detail in (4) and are required to properly monitor and control any solder process.

## Solder Profiles

**Hand Soldering.** Thermal shock in hand soldered assemblies can be the most common source of cracks and failures if care is not taken. Absolute care must be taken to insure that soldering irons are not allowed to touch an MLC termination or ceramic body, and is only used to solder MLC leads to substrates or PC boards. Figures 5 and 6

show temperature profiles for hand soldering various SMPS output filters to a PC board with capacitor sizes ranging from the smallest to largest. A thermocouple was located in the capacitor termination, near the bottom, and in the middle of the part. This was done to measure temperature changes from beginning to end of the solder process on both component sides starting on the thermocouple side. Profiles for all case sizes show temperature increases during second side soldering. Soldering was done on the opposite side of the PC board using a typical 60W soldering iron with two different tip temperatures to establish possible limitations.

Capacitor temperatures are well within allowable limits when this type of soldering is used, and there is little profile variation between different tip temperatures. Users must always be cautious when hand soldering components to PC boards to eliminate pad liftoff due to excessive temperatures and duration. Profiling hand soldered SMPS capacitor leadframes to PC boards is not required because possible part damage is remote if capacitor terminations or ceramic are not touched with the soldering iron tip.

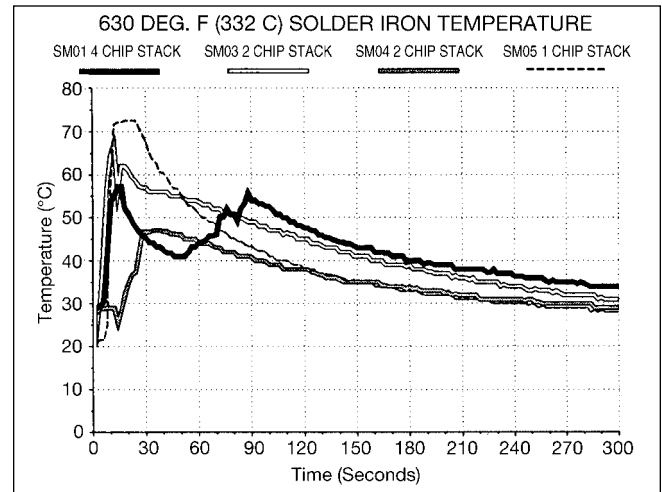


Figure 5. Hand Solder Profiles with a 630°F Tip Temperature

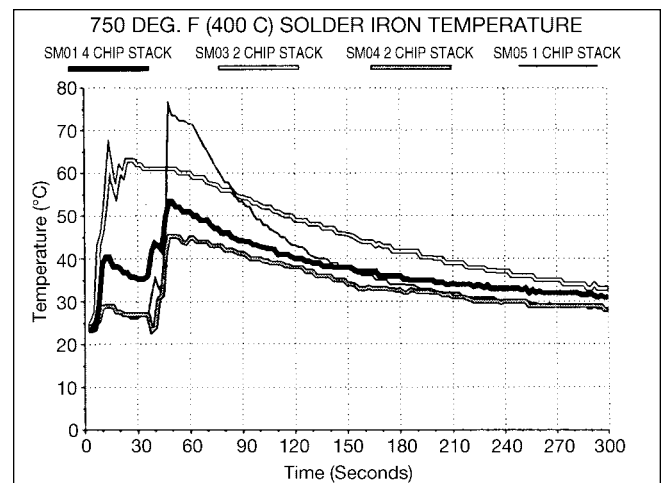


Figure 6. Hand Solder Profiles with a 750°F Tip Temperature

**Wave or Drag Soldering.** There is little chance of thermal shock damage to MLC output filter capacitors during wave or drag soldering. Capacitors and other components are isolated from the solder pot by the PC

board which minimizes heat transfer. The only potential damage that can occur is to PC boards and land pattern (pad) adhesion if exposed too long to molten solder. In each profile, thermocouples were attached to the substrate bottom to measure solder pot temperatures, to the leadframe on the top side, and foil thermocouples between the bottom chip pair and top chip pair if present. Figure 7 shows the drag solder profile of a two chip stack SM-05 (0.25" square) output filter. Slow temperature changes were measured at all capacitor points.

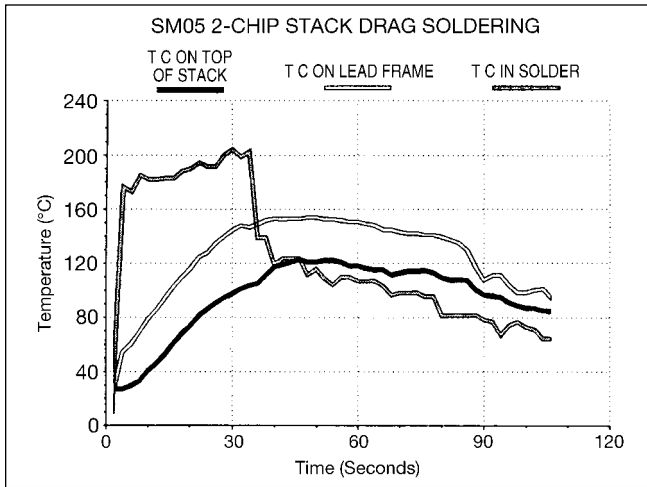


Figure 7. SM-05 Two Chip Stack Drag Solder Profile

An SM-06 (1.25" x 2.05") five chip stack is profiled in Figure 8 with four thermocouples measuring critical temperatures. As in the smaller parts case, no excessive temperatures were measured. Capacitor temperatures were lower and slower in changing due to high thermal mass of the capacitor array.

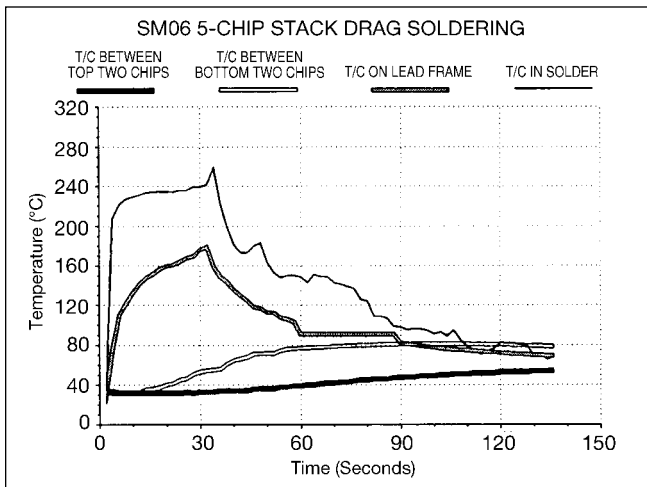


Figure 8. SM-06 Five Chip Stack Drag Solder Profile

**Infrared (IR) Reflow Soldering.** MLCs and other ceramic components are not subject to thermal shock during IR reflow soldering. This is due to low heat transfer rates and uniform heating of entire ceramic components, the termination and ceramic heat at nearly the same rate. Unfortunately large ceramic capacitors act as large heat sinks causing hot and cold spots on assemblies during

soldering. Depending on size and substrate material, areas of a substrate or some components may receive excessive heat before solder reflows on the output filter. Plastic PC boards like FR-4 and epoxy molded components such as integrated circuits or tantalum capacitors have practical peak temperatures during reflow soldering of 220-225°C. Common solders like Sn62 or Sn63 need to be reflowed at least at 200-205°C to insure proper wetting and solder joint formation. This now defines a limited process window that precludes IR reflow soldering for most large ceramic output filters larger than SM-04 (0.4" square) size. This problem is very evident in the IR reflow profile of an SM-06 five chip stack. The PC board or substrate is 3" x 5", 0.062" thick G-11 epoxy fiberglass but had a 50°C difference between the leadframe and board corner. To get solder joints on the capacitor to reflow, board surfaces isolated from the capacitor were excessively hot, delaminated, and burned. There was very little temperature difference between foil thermocouples inserted in the capacitor stack showing the heat sinking and uniform heating of large MLC capacitors during IR reflow soldering.

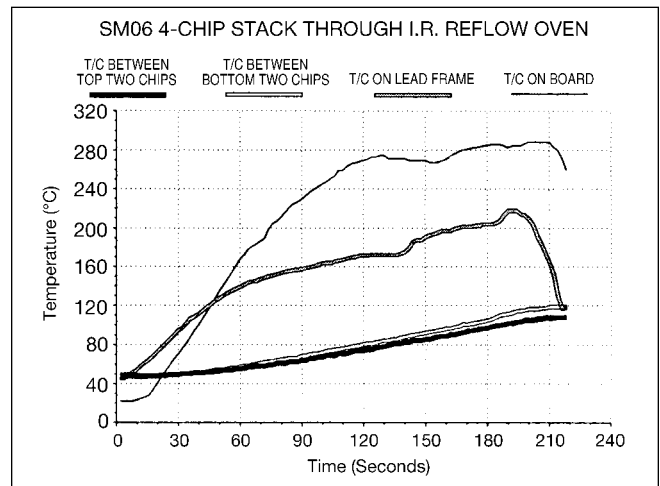


Figure 9. IR Reflow Solder Profile for an SM-06 Output Filter

**Vapor Phase Reflow Soldering.** Vapor phase is probably the most practical reflow soldering technique available today for attaching large ceramic output filter capacitors. There is some heat sinking present but not to the extent as IR reflow soldering due to constant temperature heating of condensing vapor. Peak temperatures are limited to that of condensing vapor which limits thermal exposure damage of epoxy components. One drawback is rapid temperature changes caused by the condensing vapor so without proper preheat there is a chance of thermal shock to ceramic components. Assemblies should be preheated to at least 80°C to eliminate thermal shock cracks in large ceramic and epoxy molded components. Figure 10 shows the profile on a small SM-05 with very rapid heating of the capacitor. Figure 11 is the profile for an SM-06 five chip stack but has longer temperature response due to high thermal mass. Both capacitors were on 3" x 5" PC boards and were exposed to the vapor for two minutes. Small parts like the SM-05 could

be soldered in much less time but large parts like the SM-06 needed the full two minutes to properly form solder joints. If large components are to be soldered, other component limitations may restrict these long dwell times during vapor phase soldering.

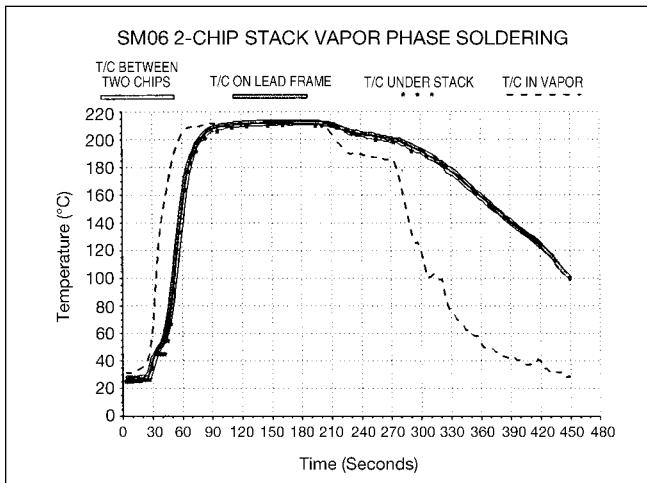


Figure 10. SM-05 Vapor Phase Reflow Solder Profile

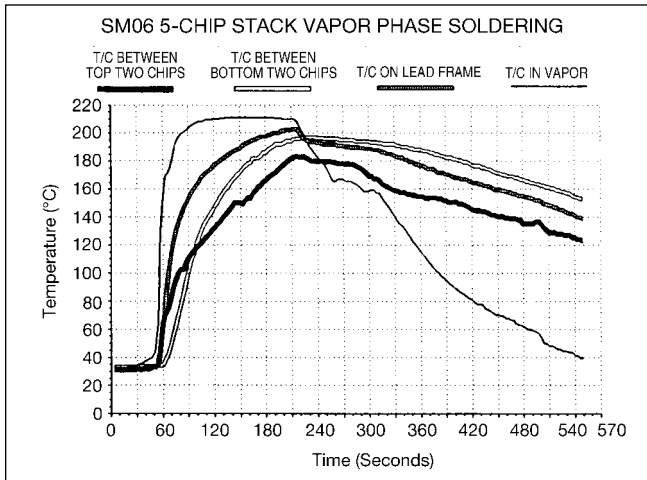


Figure 11. SM-06 Vapor Phase Reflow Solder Profile

## Conclusions

Surface mount technology and high current layout techniques will be used as high frequency switch mode power supplies move to one megahertz and beyond. There are practical SMT size limitations to components without compliant leads due to solder joint failure but adding leadframes to larger parts does not degrade electrical performance while enhancing reliability.

Component solder poses several limitations to eliminate thermal shock and substrate damage. Proper hand or wave soldering are the least damaging to capacitors because leadframes and PC boards isolate capacitors from the solder process. IR reflow soldering is not practical except for the smallest output filters due to heat sinking during reflow and excessive PC board temperatures. Vapor phase soldering may be practical for most assemblies but care must be taken to minimize damage to other components during long reflow times.

## References

1. Grover, Frederick W., "Inductance Calculations: Working Formulas and Tables," Dover, 1962.
2. Kahn, M., "Multilayer Ceramic Capacitors - Materials and Manufacture," AVX Technical Information Series, 1981, 5pp.
3. Rawal, B.S., Ladew, R., and Garcia, R., "Factors Responsible for Thermal Shock Behavior of Chip Capacitors," 37th Electronics Components Conference, 1987, pp. 145-156.



**NORTH AMERICA**  
Tel: +1 864-967-2150

**ASIA**  
Tel: +65 6286-7555

**CENTRAL AMERICA**  
Tel: +55 11-46881960

**EUROPE**  
Tel: +44 1276-697000

**JAPAN**  
Tel: +81 740-321250

**NOTICE:** Specifications are subject to change without notice. Contact your nearest KYOCERA AVX Sales Office for the latest specifications. All statements, information and data given herein are believed to be accurate and reliable, but are presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements or suggestions concerning possible use of our products are made without representation or warranty that any such use is free of patent infringement and are not recommendations to infringe any patent. The user should not assume that all safety measures are indicated or that other measures may not be required. Specifications are typical and may not apply to all applications.

  
[WWW.KYOCERA-AVX.COM](http://WWW.KYOCERA-AVX.COM)