TECHNICAL INFORMATION

ASSEMBLY INDUCED DEFECTS

by John Maxwell
AVX Corporation

Abstract:

Surface mount technology holds many benefits but there is no room for sloppy practices; SMT assemblies need the control that semiconductor processing uses. Extreme care must be taken at the start of a design to identify all stress zones and orient components to minimize damage.

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Introduction

The transition from thru-hole manufacturing to surface mount technology has made one thing crystal clear: surface mount components and PC boards are easily damaged by the soldering and assembly process. Multilayer ceramic capacitors are sensitive components to damage due to their complex mechanical structure. But experienced users are now finding out the hard way that PC boards, plastic molded ICs or transistors, and even solder places stringent limitations on assembly processing. The entire assembly is now subjected to the soldering process exposing all components and the PC board to high temperatures for long periods of time. Unfortunately some materials, in particular the plastics used to manufacture SMT components and PC boards, are not well suited for high temperature processing. Sources of assembly induced damage fall into two major categories: thermal and mechanical.

Thermal Damage

Damage to PC boards, plastic molded components, and solder is primarily thermal in nature while chip capacitor and resistor damage is mostly due to external mechanical stress. Thermal shock cracks in ceramic capacitors have been described in detail as to causes and solutions (1, 2). Users are now discovering post solder cracks in plastic IC packages (3), and PC board blistering, measles, or delamination. The main culprits are moisture absorption by the plastics and stress due to large differences in the coefficient of thermal expansion (CTE) of materials used by the manufacturer of plastic molded components and PC boards.

When processing temperatures exceed the glass transition temperature, Tg, of epoxy resins, the CTE can increase as much as an order of magnitude over room temperature values further increasing stress.

Common vapor phase or infrared reflow soldering temperatures are far beyond the boiling point of water or glass transition temperatures of epoxies used in PC boards and molding compounds. A user can do very little to minimize stress due to CTE mismatch other than follow a supplier's recommendations on process limitations. These usually include peak processing temperatures and maximum rates of change, dwell times, and preconditioning procedures.

Material preconditioning is used to drive moisture out of epoxy resins using time and temperature. A common solution recommended by both suppliers of ICs and PC boards is to bake both for extended periods of time at 125°C for 8 to 24 hours. Unfortunately, solderability of components and PC boards degrades rapidly at these times and temperatures due to intermetallic consumption of tin in the solder plating of base metals. Solid state diffusion of tin and the base metal forms the intermetallic layer needed for solder joint formation, but once the tin is completely consumed, a nonsolderable surface remains. Tin copper (4) is the fastest forming intermetallic compound at temperatures below 150°C, right in the range of board and component preconditioning temperatures. If component lead or board trace plating is too thin, there will be solderability problems in the production process. These problems are compounded by the move to fine pitch IC packages and the necessary reduction in plating thickness on the leads.

Table I. CTEs of Typical Components and Substrates

Material	CTE(ppm/ºC)
Chip Capactior	9.5-11.5
Chip Resistor	≈7
Copper	17.6
FR-4 PC Board (X<Y)	≈18
Filled Epoxy (<Tg)	18-25
Kovar	5.3
Tin Lead Alloys	≈27

Solderability testing of components and PC boards in the intended solder process is the only test users have to see if preconditioning has rendered components or PC boards unusable. A reflow solder process cannot be constantly adjusted to accommodate poor solderability due to other material limitations. Once a process is established, all components used must be solderable.

Common solders like Sn62 or Sn63 used in SMT assemblies impose their own limitations (5, 6) on thermal exposure. There are two fundamental limitations imposed by solder: first, solder exposure above the liquidous temperature needs to be minimized; and second, solder joint exposure to high temperatures also needs to be minimized. The first is due to reflow soldering limitations imposed by plastics used in the PC board and molded components. These materials limit practical assembly peak temperatures to 220-225°C which is below the melting point of all the elements in solder with tin being the lowest at 232°C. Even though the solder alloys melt at 183-186°C, exposure to temperatures below the melting point of tin promotes the formation of lead dendrites in the solder. The separation of tin and lead in liquid solder increases the solder grain size when the solder joint freezes, reducing strength and reliability. Soldering assemblies for longer periods of time only degrades solder joint reliability, epoxy molded components, and PC boards. Once a solder joint has formed, the soldering job is done.

The second solder limitation relates to grain structure deterioration after the solder joint is formed. Grain structure changes are minimized when solder joint temperatures are kept below 125°C but change rapidly above 135-150°C. Again, there is separation of tin and lead, and enlarged grains reducing solder joint strength and reliability. This is usually not a concern during normal operation unless components are dissipating large amounts of power.

Typically excessive post solder joint heating occurs at later steps in the production process such as wave soldering components to PC boards while using excessive preheat, hand soldering large components or RF shields, or "NUKING" boards during rework/repair.

Rework/repair is the most common cause of excessive solder joint heating. Usually large, hot soldering irons or overblown hair dryers are used in this process not only removing the desired parts but also destroying PC land pattern adhesion and degrading adjacent solder joints. When excessive heating occurs, premature failure results in erratic electrical behavior early in the product life. Sometimes these failures are found during product test if thermal cycling is performed, but the majority of failed solder joints are found by customers. Fractures in fatigued solder joints occur in high stress zones and are due to differences in CTE, component length, and temperature excursions. Figure 1 shows typical solder joint stress zones for chip components and PLCC IC packages. Other SMT components such as SOICs (small outline IC), quad chip carriers, SOTs (small outline transistor), inductors, and tantalum capacitors all have similar joint stress zones.

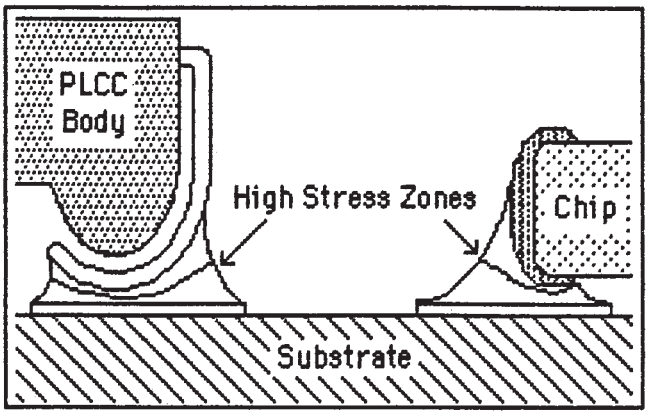

Figure 1. Solder Joint Stress Zones

Longer components have larger solder joint stress during temperature cycling due to larger linear displacement. Linear displacement is the difference in length of a component and the segment of substrate between solder pads during temperature excursions. Linear displacement is:

$\Delta L = (L)\ (\Delta CTE)\ (\Delta T)$, where
L is the initial segment length
ΔCTE is the difference in component and substrate CTE
ΔT is the temperature excursion

Figure 2 shows linear displacement for both PC boards where the CTE is greater than that of a component and a ceramic substrate where the opposite is true.

Solder joints of large components like IC packages are the first to fail due to high temperature exposure. Failures typically occur at package corners which are the highest stress areas due to large linear displacement. Extreme care must be taken during all rework/repair process stages to minimize adjacent solder joint temperatures. It is not uncommon to find 80W soldering irons in these areas because production managers want to get things done quickly, and speed in soldering requires both high power and temperature. Some large components require a great deal of heat to be soldered because of high thermal mass so they should be physically isolated from other solder joints

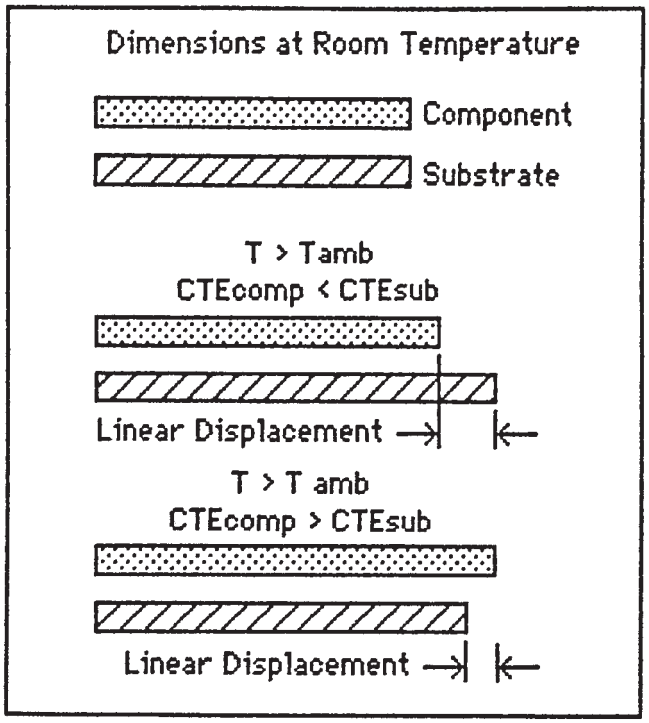

Figure 2. Linear Displacement for Different Substrate Conditions

by design so their installation does not degrade reliability. In particular, large IC packages need to be isolated from excessive heat because a solder joint failure will usually crash the system, but the loss of a chip capacitor or resistor may not. Adjacent solder joint temperatures must be limited to less than 125-135°C or there will be latent failures.

Mechanical Damage

The old pat answer that all cracks are due to thermal shock is no longer true for ceramic capacitors and resistors, as pick and place machine damage and post solder assembly handling are now the major sources of induced damage. Thermal shock can and does occur, but only when parts are wave soldered with little or no preheat or "NUKED" with large soldering irons during repair/rework procedures.

From 1983 to 1988, pick and place machines were the dominant source of induced damage with thermal shock and post solder handling making up the balance. Since 1988, there has been a shift to post soldering damage as the primary induced source due to improvements in three areas. Capacitors have improved, both wave solder users and equipment vendors recognize the importance of proper preheat, and there have been advances in pick and place machine component alignment mechanisms. All induced defect sources may be present at one time along with the possibility of defective components masking those sources. With the exception of placement damage, thermal shock and post soldering damage will cluster in specific areas on an assembly. Unfortunately placement damage like defective incoming parts are randomly distributed across the board requiring detailed failure analysis including DPA (destructive physical analysis). Each source of damage has a unique crack signature that helps identify the cause helping manufacturing to eliminate those defect sources. Pick and place machine and post solder handling damage are the major defect sources facing users today and will be covered as separate topics.

Pick and Place Machine Damage

Placement damage falls into three categories: top mechanical alignment or centering, bottom centering, and placement cracks. Bottom centering is the least common type of damage today for two main reasons. First, the centering jaws are low mass and do not impact parts as hard as do high mass top centering jaw machines. Second, paper tape packaging has improved or been replaced with plastic embossed carrier tape minimizing debris in the centering jaws and associated misalignment damage. Only vacuum pick-up bit and top mechanical centering will be discussed.

Vacuum Pick-up Bit Damage. Damage or cracks caused by vacuum pick-up bits is straightforward but perhaps not quite so obvious. This type of damage is caused by excessive Z-axis placement force of the vacuum pick-up bit during component placement and consists of damage typically just below the surface. In the case of MLCs the damage typically occurs at the ceramic cover layer/electrode interface on the chip interior, and from the top surface it looks like the ceramic is disturbed in a circular- or halfmoon-shaped area. Most ceramics used in making MLCs are translucent so cracks 5 mils or so below the surface can look like an impression. In some cases there will be surface fractures but this has become less common. Another manifestation of bit damage occurs where solder paste is on boards supporting parts only on their terminations. Tensile rupture cracks may be found on the component bottom or board side running from side to side in the middle of the part, These internal or surface cracks lead to excessive leakage currents and capacitor failure.

Chip resistors receive similar damage but surface chip outs or cracks in the resistive element will result in erratic resistor values. Time and power/temperature cycling are needed to promote failure. Figure 3 shows placement bit damage for both chip capacitors and resistors.

Placement bit damage is the result of excessive placement force because of improper machine maintenance, set-up, or equipment failure. Plant air pressure variations,

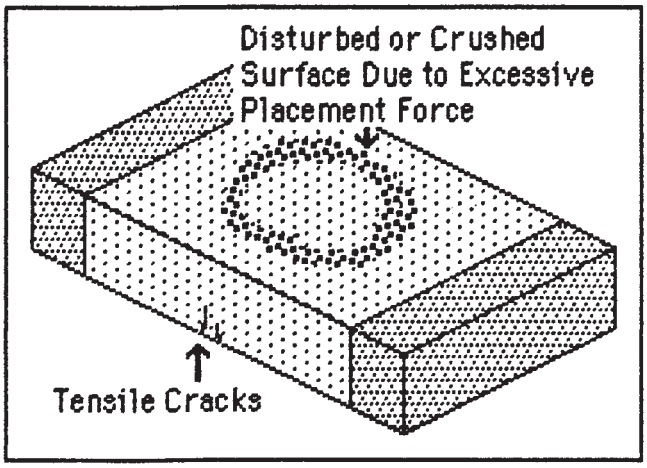

Figure 3. Common Placement Bit Damage

dirt or water in air lines, and age make it difficult to maintain consistent placement force. It is uncommon to find two pneumatic driven pick and place machines with the same pressure settings within the same facility. Placement force or pressure is a process parameter that needs to be monitored on a by-shift, by-machine basis. Machines with programmable placement pressure also require placement force monitoring on a daily or shift basis because of the possibility of force sensor failure. When in line monitors are used, machines are set up the same way insuring consistent assembly quality. It's best to eliminate problems in the production line by process control.

Top Centering Jaw Damage. Top centering jaw pick and place machines use alignment jaws or tweezers as part of the pick-up mechanism such that the part is centered when plucked from the component carrier (embossed tape, etc.) or during travel to the placement location. Capacitors, resistors, transistors, and integrated circuits all require different sizes of jaws and centering forces for optimum placement. Unfortunately production requirements may not allow jaw changes, forcing a compromise where a single jaw set is adjusted to accommodate large ICs, subjecting smaller parts to excessive forces. Not only are high forces present but most centering jaws have small widths, especially on the ends, increasing alignment stress. Transistor and integrated circuit plastic bodies are used for alignment instead of the leads to minimize lead bending, concentrating stress into the top 10-20 mils of small parts. MLC capacitors have a tensile strength of ≈10,000 psi and a compressive rupture strength of ≈15,000 psi. These numbers seem high until we realize that a phonograph stylus exerts similar forces on vinyl records. The actual gram force or pound force exerted by centering jaws must be minimized to eliminate these defects. Figure 4 shows force concentrations due to mechanical centering jaws. Figure 5 shows typical visible top centering jaw cracks.

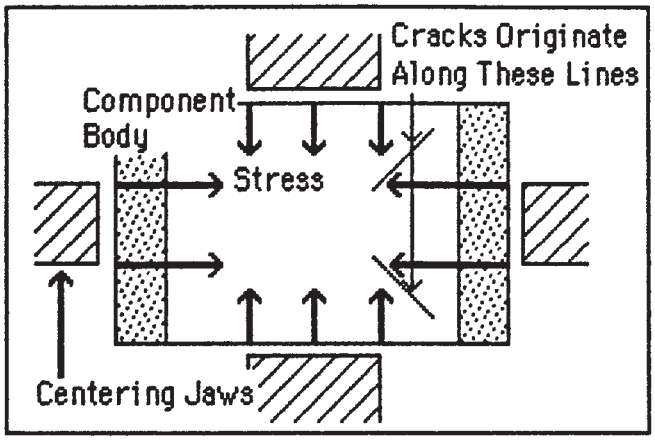

Figure 4. Component Top View of Centering Jaw Force Concentration

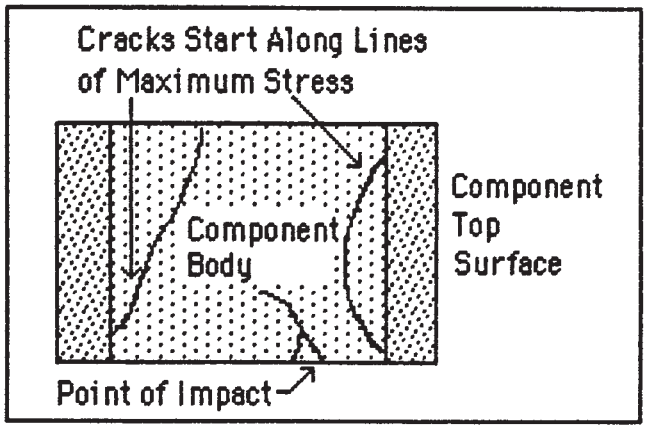

Figure 5. Resulting Visible Top Surface Cracks

Most induced damage from any source is not visible but is in the interior of the part or hiding under the termination. It's not uncommon to find 90-95% of the damage hidden from view so when the visible cracks disappear the job is not done. Impact fractures are typically located 10-15 mils from the top surface hidden under the termination as shown in Figure 6.

This type of internal crack does not fail quickly because there are no cracks that propagate to the surface which allows entry of external contaminants such as moisture or flux. It has been shown by Brannon, et al. (8) that atmospheric moisture and DC voltage are all that is required to initiate the onset of leakage current in MLCs. Water hydrolyzes at DC voltages above 0.87V providing an electrolyte needed for current conduction which occurs very quickly, causing a failure. Internal cracks require metal dendritic growth or precipitation between electrodes taking some time before the onset of leakage failures.

There is a very insidious form of internal damage that manifests itself as a single inter-electrode crack between only two or three electrodes that is initiated during centering. Figure 7 shows this type of crack and exaggerated ceramic distortion during impact. Again these cracks exist 10-15 mils below the top surface, right along the impact plane of the end centering jaw, and 5-15 mils from the termination.

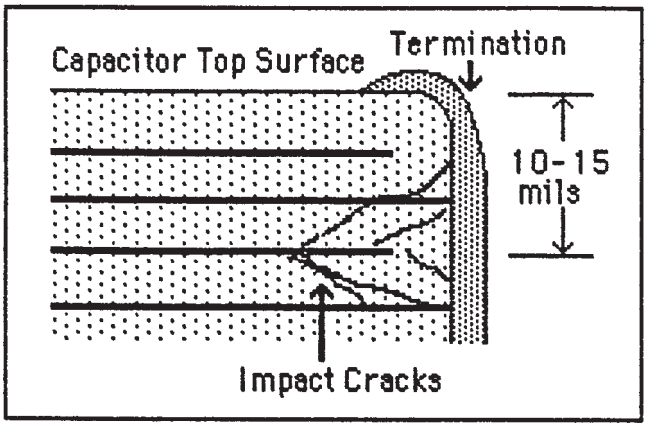

Figure 6. Internal Centering Damage

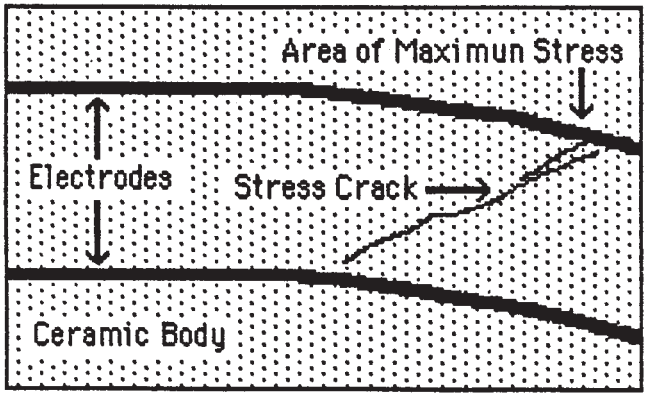

Figure 7. Inter-Electrode Impact Crack

Centering jaw damage will be with us until mechanical alignment is replaced with vision systems and computer-corrected placement. Equipment manufacturers and users have recognized that pick and place machines are a major source of damage and are taking steps to eliminate it. Post solder handling will be the major source of induced damage facing component users in the future.

Post Solder Handling Damage. Post soldering or uncontrolled warping after soldering is the least recognized form of induced damage in surface mount assemblies. Warping or bending occurs at many process steps after soldering. Board test, component or connector installation, depanelization or singulation from a mother board, and final product installation are the most common sources of post solder cracks. In each case of these cracks, the tensile strength of the ceramic is exceeded. These cracks do not need thermal processing such as soldering to propagate but occur with an audible snap.

Solder joint mass has an effect on when cracks occur. Large, bulbous solder joints transfer most bending stress to the component instead of stretching to relieve stress, making an assembly more sensitive to handling. Allowable bending of finished assemblies is a specification that cannot be an extension of thru-hole technology because entire components are exposed to stress. There are two possible approaches to board bending specifications: a linear mils/inch, or a more realistic minimum bend radius (7).

Minimum bend radius allows only a small deflection in short segments but a great deal of deflection in long segments. For example, a one-inch long segment can have no more than 8.4 mils of uniform deflection with a 60- inch minimum bend radius, and increases to 124 mils for a four-inch segment. Uniform bend or deflection is where the board fits smoothly along the radius of a circle. If there are large rigid-like ICs, transformers, or connectors, then less deflection is allowed for any given board length. They key to eliminating warp cracks is to minimize board flexure at all handling and installation steps after soldering components into place.

Manufacturing efficiency dictates multi-up or multiple assembly panels but here lies the single biggest source of warp cracks. Singulation or depanelization processes can induce a great deal of stress (board flexure) in components near board edges and corners. There are many techniques available to depanel mother boards, some generate excessive stress. High stress and usable processes are listed in Tables 2 and 3.

Table 2. High Stress Depanelization Techniques

1) Prescored boards
2) Perforated boards
3) Routing
4) Breakout tabs
5) Shearing including blanking shears

Table 3. Usable Depanelization Techniques

1) Shearing prerouted boards
   a) Components must be isolated from shear tabs
   b) Rigid fixturing
   c) A very fast process
2) High speed fine tooth saws
   a) Limited only to linear cuts
   b) Rigid fixturing is mandatory
   c) A dust and debris cleaning step is required
   d) A medium speed process
3) Diamond wire cutting
   a) A dust and debris cleaning step is required
   b) A slow process
4) Laser cutting
   a) Currently is limited to 0.047"-thick PC boards due to excessive board edge charring

b) Conductive carbon tale cleaning step is mandatory
c) It's expensive and slow

5) Water jet
a) Slow
b) Expensive
c) An additional cleaning/drying step is needed

Cracked components from any board warping source all have the same signatures. There are two basic failure modes depending on how the board is bent and if solder mask is present or not. The presence of solder mask between component pads makes an assembly more sensitive to handling damage. Coplanar parts like chip capacitors, resistors, and transistors will solder flush with the pads due to molten solder surface tension forces. Now the component body is resting on solder mask which acts as a fulcrum, increasing component stress. Depending on board warp, direction, and component orientation, these cracks propagate to relieve mechanical stress. Cracks initiate at the ceramic termination interface where ceramic movement is restricted by the termination and solder fillet. Because materials fail more readily in the tensile mode, crack initiation will typically be at maximum tensile stress sites as shown in Figure 8.

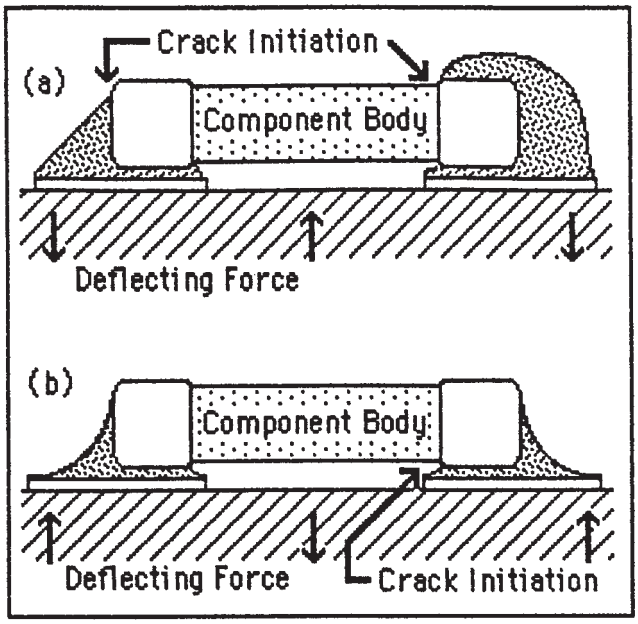

Figure 8. Crack Initiation Sites

Board warp cracks propagate at a 45° angle away from the initiation site. When DPA is done on failed units, failures are often confused with thermal shock or pick and place machine damage. Thermal shock cracks are at the top surface and usually consist of a single crack. Pick and place machine damage is typically under the termination with multiple fractures and warp cracks always originate at the top or bottom ceramic/termination interface angling in toward the component end. Figure 9 shows typical fractures in both capacitors and resistors. Chip resistors pose an interesting problem in that they are cut from a piece of ceramic resulting in sharp corners. This makes them more sensitive to cracking terminations than MLC capacitors which have rounded corners and edges. There is greater stress concentration at sharp corners than ones that are rounded which increases component sensitivity to board warp.

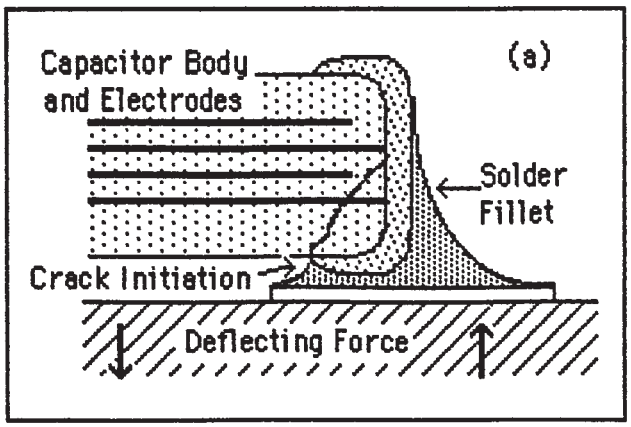

Figure 9(a). Typical Board Warp Cracks

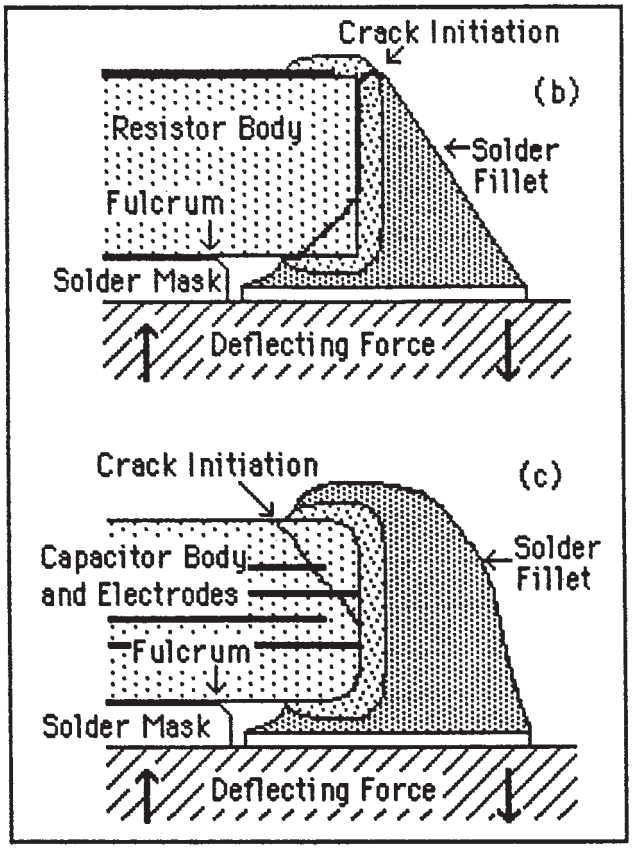

Figure 9(b, c) Typical Warp Cracks

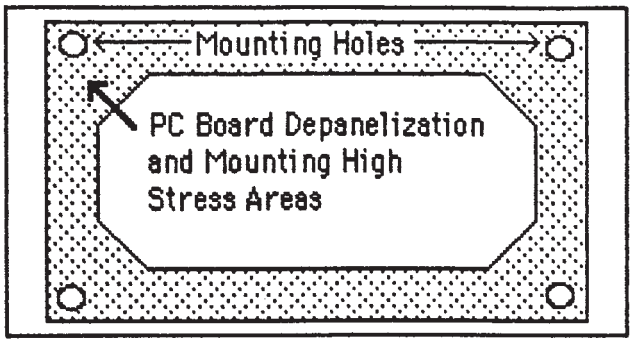

Figure 10. Typical High Stress Zones for Mounting and Depaneling

There are regions on boards that experience too much deflection to achieve high yields and reliability. Rigid components like capacitors, resistors, and transistors need

to be isolated from these flex or warp zones which are greatest near mounting holes, connectors, pots, transformers, and other large parts. Board edges or corners receive the greatest warp or stress during handling and installation so components should be isolated by at least 200 mils from those areas. Figure 10 shows typical high stress zones for depanelization and mounting holes. Each assembly will have different areas to be avoided and in some cases are so complex that common sense won't work. Finite element analysis, FEA, programs are now available for personal computers and should be used in the initial design so high stress 'zones are identified and sensitive components are isolated before there are production defects.

Conclusions

Every step in an SMT assembly process can induce defects. Sub ppm defects demand these potential sources be identified and eliminated. The tendency to "use a bigger hammer to make it fit" syndrome will only damage SMT assemblies. Force fitting a process or boards will only damage components, causing field failures. Surface mount technology holds many benefits but there is no room for sloppy practices; SMT assemblies need the control that semiconductor processing uses. Extreme care must be taken at the start of a design to identify all stress zones and orient components to minimize damage.

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