TECHNICAL PAPER

Increasing Reliability of SMD Tantalum Capacitors in Low Impedance Applications

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Abstract

High dv/dt conditions in low impedance circuits using surface mount tantalum capacitors is discussed. Circuit designs utilizing low $R_{(DS)ON}$ MOSFETs for preventing these conditions are presented in detail.

INTRODUCTION

Reliability over time, temperature stability over the range -55 to +125 degrees C, high volumetric efficiency, and low ESR has lead to the solid tantalum capacitor being the dielectric of choice for decoupling, bypass and filtering applications in the (10-330) microfarad range. Many applications for the higher capacitance values will have low circuit impedances and will require the designer to have an understanding on the strengths and weakness of tantalum capacitor technology. In low impedance applications, current in-rush is always a concern and has typically been controlled by the inclusion of external series resistance in the circuit to promote self healing.[1,4] A high current in-rush application is defined as one where over one ampere of charging current is available to the capacitor.[2]

The recommended series resistance for solid tantalum capacitors in low impedance applications in the late fifties and sixties was three ohms per working volt to ensure standard operational component level reliability. The three ohms per working volt was empirically determined as the amount of resistance required to prevent breakdown caused by "scintillation" (momentary dielectric breakdown).[3,4] This additional amount of series resistance was not critical due to the low frequency applications where tantalums were used. Filtering at 120 Hz for a 100µf capacitor yields a reactance of about 13 ohms. A few ohms of series resistance in this application was not critical.[3] Typical switching frequencies in DC-DC converter applications today can range from a few kilohertz to the megahertz range. The same capacitor used at 100 KHz has a capacitive reactance of approximately 15 mOhms. The ESR of the capacitor is a larger contribution to impedance than the capacitive reactance. Addition of a few ohms of resistance is not possible if the capacitor is to be application effective. Here the additional resistance would reflect a measurable contribution to the loss in efficiency of the circuit.

By the seventies and eighties these recommendations for steady state applications had reduced to one ohm per working volt. Today, KYOCERA AVX references one hundred milliohms per working volt for standard steady state reliability on all of its tantalum product lines. These changes are a direct result of advances in manufacturing processes and increases in the purity of capacitor grade tantalum powders. However, these recommendations are for steady state conditions within circuits and do not directly address dynamic conditions (i.e. voltage and current transients).

With the advent of surface mount technology and the associated closer interconnection distances, the actual series resistance available in applications has reduced, making transients an even more important consideration. When tantalum capacitors are used in such low series impedance applications they are subject to large current in-rushes, especially if the source supply is of low impedance. During initial testing of assemblies, this environment can produce a low, but measurable PPM (Parts Per Million) fallout of early life failures under certain circuit conditions.

In the following sections, this failure mode and the conditions under which it can occur are defined. The component level solutions being employed by manufacturers are also reviewed and alternative design level solutions are introduced and discussed.

COMPONENT LEVEL SOLUTIONS

The construction and manufacture of tantalum capacitors is well defined within several industry papers referenced in the bibliography [1, 3, 5, 12]. The construction of the tantalum capacitor element is such that the tantalum pentoxide dielectric is operated under a high degree of electrical stress.

This can best be understood with reference to the construction of the part. A typical 22 microfarad device capacitor rated at 20 volts has a dielectric

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layer thickness of less than 1 micron and a dielectric area of 150 square centimeters. This gives rise to a field strength (steady state) of 147 kilovolts per millimeter.[6] By preconditioning the capacitor to a low impedance current surge while maintaining maximum dielectric stress, a certain degree of control over later surge susceptibility can be achieved. Most manufacturers have now incorporated current surge testing to accelerate any infant mortality or latent defect failures in their product. Surge test is an important assessment of the dielectric quality.

Typical current surge testing on capacitors is performed by charging a large bank of electrolytics to the working voltage of the capacitor, and then discharging the bank through a low$R_{(DS)ON}$ FET to the device under test. The FET prevents contact bounce commonly seen in relay or mercury switch operations. If the component were to be exposed to contact bounce the average RMS of the current would be decreased by the open contact periods. The most important aspect of eliminating contact bounce is to ensure that the maximum peak current is delivered to the device under test. The amount of current the capacitor will see depends on the impedance of the test setup. A total impedance of one to two ohms is common. This impedance comprises the cable resistance, contact resistance, interconnections, and inductive reactance of the supply cable. In order to verify a part receives the correct amount of surge current, a current sense resistor and monitoring circuitry is typically incorporated into the test setup.[5]

Component Choice and Surge Resistance

One of the factors affecting the peak current developed in the capacitor is the intrinsic equivalent series resistance (ESR). When considering the peak current delivered in a given application or test, this must be taken into consideration.

Assume a 22 microfarad component rated at 25 volts is subjected to a surge test similar to the one previously described. The KYOCERA AVX TPS low ESR product line has a maximum ESR of 0.200 ohms at 25 degrees C. The standard KYOCERA AVX TAJ component has a maximum ESR of 0.900 ohms at 25 degrees C. Therefore the following are received by each component using a 1 ohm impedance for the test setup resistances.

TPS

I_{Peak} = E / Z

We can generalize and say that Z = R for this example.

I_{Peak} = 25 volts / (ESR) + R_{Cable}
I_{Peak} = 25 volts / 1.2 ohms
I_{Peak} = 20.83 amps

Standard TAJ

I_{Peak} = E / Z
I_{Peak} = 25 volts / 1.9 ohms
I_{Peak} = 13.15 amps

The inductive component for the leadframe of the capacitor is approximately 3 nanohenries and can be neglected for the purpose of this example. The time constant for the surge will be the product of the capacitance under test and the impedance of the test setup. To quantify, we are typically looking at 10µ to 330µ seconds depending on capacitor value. This brings up another dilemma that the test engineer faces when implementing current surge testing. The smaller the capacitor the shorter the time constant. The shorter the time constant the shorter the voltage rise time has to be in order to deliver the maximum surge possible.

Surge Considerations in Specific Applications

As can be seen from the above illustration, there is a significant difference in the exposure level between standard and low ESR components when subjected to current stress screening. The magnitude of the surge each component receives is inversely related to the component's ESR. Capacitors should be surge tested individually for this reason. If the components were placed in parallel for surge testing, the variation in ESR between the individual capacitors and the amount of trace inductance/resistance between each will distribute the current unequally. By surge testing

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individual parts, this variation is reduced which gives a greater level of consistency in the maximum surge received by each part.

When these components are placed into a circuit with no series resistance and the source is of low internal impedance, the only limiting factors affecting the amount of current available are the interconnection resistances, the internal impedance of the source (or linear regulator, switcher, etc.), the trace resistances, and the capacitor ESR. A worst case example of what the same capacitor could see in the low impedance input circuit of a notebook computer is as follows:

Capacitor Resistance	200 mohms
Nickel-Cadium Battery (D1)	35 mohms
Board Trace resistance	15.0 mohms
Battery Contact Resistance	10.0 mohms
Total	260.0 mohms

A fully charged battery pack of 10 vented sintered plate Nickel-Cadium batteries (standard D cell) would have a open circuit voltage of 12.5 volts when fully charged.[7] Nominal operating will be 12.0 volts. Total internal resistance will be approximately 35 milliohms (3.5 x 10). The variation in series resistance among different Nickel-Cadium configurations is large and contributable to differences in cell design and packaging. Using the approximate figure of 300 milliohms for all resistances would result in possible current in rush of 40.0 amps at initial turn on.

$$I_{MAX} = 12.0 \text{ volts} / 300 \text{ mohms}$$
$$I_{MAX} = 40.0 \text{ amps}$$

The only limiting factor is the 300 milliohms resistance of which the capacitor ESR is the main contribution. This means that the initial power dissipation (energy loss) of the circuit for the current in-rush condition will be predominantly from the capacitor ESR. This magnitude of current in-rush far exceeds any current in-rush test performed in mass production facilities today and reinforces the need for implementing current in-rush precautions. A list of possible operational conditions where this scenario could occur is provided in the DC-DC Converter Input Filtering section.

As a general note, adding multiple capacitor components in parallel will assist in operational ripple current sharing provided that track resistance and inductance is minimized. But adding multiple parallel capacitors will also decrease the effective ESR of the capacitor bank allowing higher peak currents from the supply source. The amount of current each capacitor in the bank will see depends on its individual ESR.

The use of Low ESR Capacitors increases the amount of ripple current the capacitor can handle for the same case size power rating and will also provide lower ripple voltage output than standard components. But the intrinsic lower ESR also allows for higher current inrush conditions when subjected under the same conditions as standard components.

DC-DC Converter Input Filtering

The primary failure location of tantalum capacitors when used in a power supply application is the input side of the regulator or converter. This is primarily due to the capacitors exposure to an uncontrolled energy supply of low impedance. The dv/dt the output capacitors will see is typically a function of the “soft start” of many converters. It is common to take several cycles for a switch mode power supply to ramp up to the intended output voltage. The inductor in series with the output capacitors in many topologies also ensures that current in-rush is limited to the output capacitors.

To better understand how input capacitor failures occur, we need to evaluate the response of a step function on the input circuit. A capacitor subjected to a high dv/dt can have its dielectric damaged. Once the dielectric is damaged, normal operating conditions (high ripple at elevated temperatures) will allow rapid breakdown of the capacitor. The ability of the capacitor to self heal momentary breakdown of the dielectric is nonexistent in low impedance circuits.[2] We can use a simple series/parallel circuit to demonstrate the minimum allowable rise/fall time for prevention of large current transients. First, we will develop the circuit using a realistic application.

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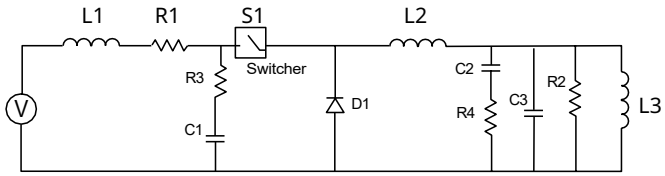

Figure 1 - Typical Switch Mode Power Supply

In a typical switch mode power supply (Figure 1), when power is initially applied, the source sees the circuit as having track inductance, track resistance, and the capacitor ESR. Typically the switch will not turn on until the voltage increases to a preset trip point. With the switch in the off mode all energy is diverted into C1 (the input capacitor). The initial turn on generates damped oscillating transients with self resonant frequencies.

L1 = Lump Sum of Track Inductance and Battery Inductance
R1 = Lump Sum of Track Resistance and Source Resistance
C1 = Input Capacitance
R3 = Capacitor C1 ESR
S1 = Switch
D1 = Switcher Diode
L2 = Output Inductor
C2 = Output Filter Capacitance
R4 = Capacitor C2 ESR
C3 = Output Load Capacitance
R2 = Output Load Resistance
L3 = Output Load inductance

We can simplify this schematic by applying a voltage source with varying rise time and combining similar component properties. Figure 2 is the result.

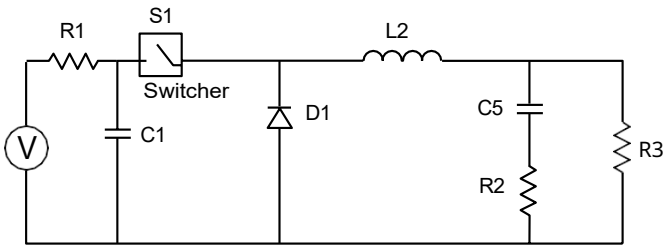

Figure 2 - Simplified Schematic

C1 = Input Capacitance (22µ F)
C5 = Output Capacitance (220µ F)
S1 = Switcher
D1 = Switcher Diode
L2 = Output Inductance
R1 = Combined Resistance (Input Capacitor ESR and Track Resistance)
R2 = Combined Resistance (Output Capacitor ESR and Track Resistance)
R3 = Output Load Resistance

Evaluating the circuit mathematically is now straight forward. For our simulation, we are using a 47 microhenry output inductor with a 220 microfarad output capacitor with a maximum ESR of 100 mohms.

An approximation of 300 mohm can be used to simulate ohmic resistance through the capacitor, inductor, and track.

We will now focus on a step function of 12 volts using different dv/dt rates. This input is applied across the input capacitor to simulate the effect various dv/dt has on current in-rush for the tantalum capacitor. We can do this through modeling in SPICE. The following SPICE model was used for the emulation:

```
Simplified Circuit
.PRINT TRAN V(2) V(3) V(4)
.PLOT TRAN V(2) V(3) V(4)
.TRAN 10NS 900US
.PROBE
C1 2 0 22UF
R1 2 1 0.300OHMS      ; Combined Resistance
R99 2 0 99999GOHMS ; Dummy resistors to prevent
                      capacitor C1 from floating
R98 4 3 99999GOHMS ; Dummy resistors to prevent
                      capacitor C5 from floating
D1 0 2 D1N4148        ; Generic Diode for modeling
L2 2 3 47UH
C5 3 4 220UF
R2 4 0 0.300OHM       ; Combined Resistance

V1 1 0 PULSE 0V 12V 1US 100NS 100NS 2S 5S
    ; Format is V1, V2, Delay Time, Rise Time, Fall
    ;Time, Pulse Width, Pulse Period
.MODEL D1N4148 D (CJO=5PF VJ=0.6 M=0.45
RS=0.8 IS=7E-9 N=2 TT=6E-9 BV=100)
.END
```

(The switch is assumed closed for the analysis.)

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This simulation model will show us the mathematical relationship of i = c dv/dt in the circuit. This graphic illustration clearly shows the importance of controlling the dv/dt on the input capacitors.

The 100 nanosecond rise time plot: $I_{MAX} \cong 40$ amps

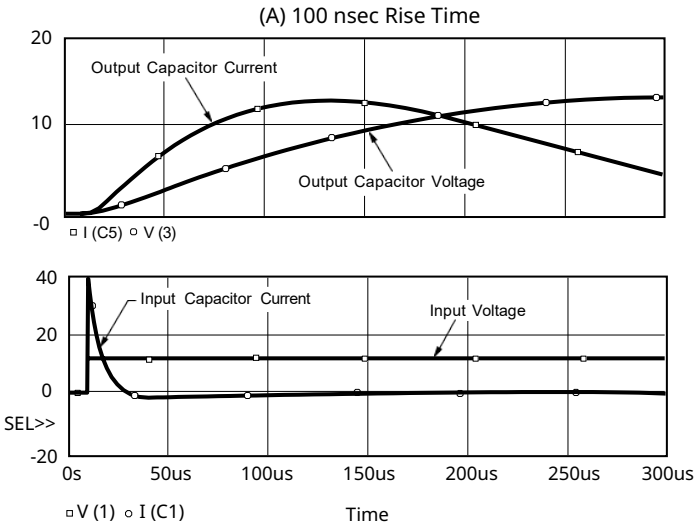

Figure 3 - 100 Nanosecond

As you can see the circuit experiences a large current in-rush due to the rise time of the waveform. The later graphs will show a decrease in peak current excursions as the rise time increases on the input voltage. The 12 volt step function is obtainable under several different conditions within a notebook computer. Some of those conditions are:

1. When a battery charging unit (AC-DC adapter) is plugged into the wall outlet prior to connection of a unit containing no battery, input capacitors could be subjected to an input voltage of 20-24 volts.

2. 1. When a battery charging unit (AC-DC adapter) is plugged into the wall outlet prior to connection of a unit containing a battery, input capacitors could be subjected to an input voltage increase of 8-12 volts.

3. When the battery charging unit is plugged into the computer prior to plugging into the wall, the energy stored in the notebook computer input capacitors could be transferred to the large low ESR reservoir capacitors on the output of the AC-DC adapter. This is possible if the series resistance of the battery and its associated connective paths are more than the notebook input capacitors.

4. When a battery is removed and replaced after the capacitor has had time to discharge.

The above conditions represent realistic possibilities where the capacitors are either partially charged or are starting from zero potential. The result is the same, a delta in voltage potential that influences the in-rush current of the circuit.

The 10 microsecond rise time plot: $I_{MAX} \cong 20$ amps

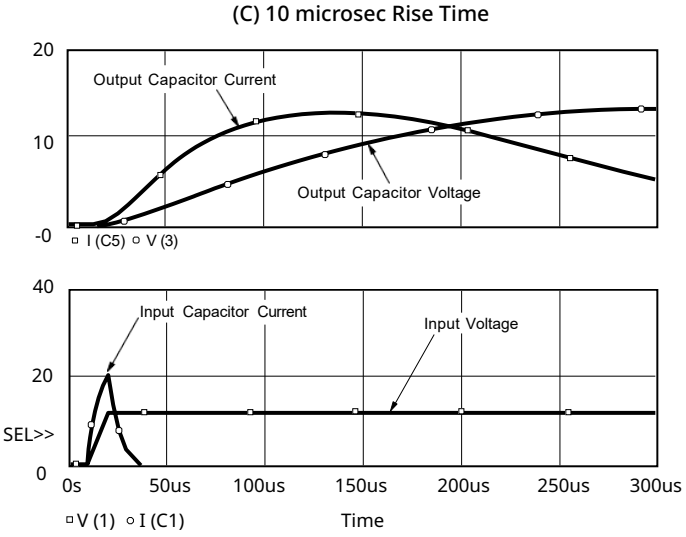

Figure 4 - 10 Microsecond

The 15 microsecond plot: $I_{MAX} \cong 16$ amps

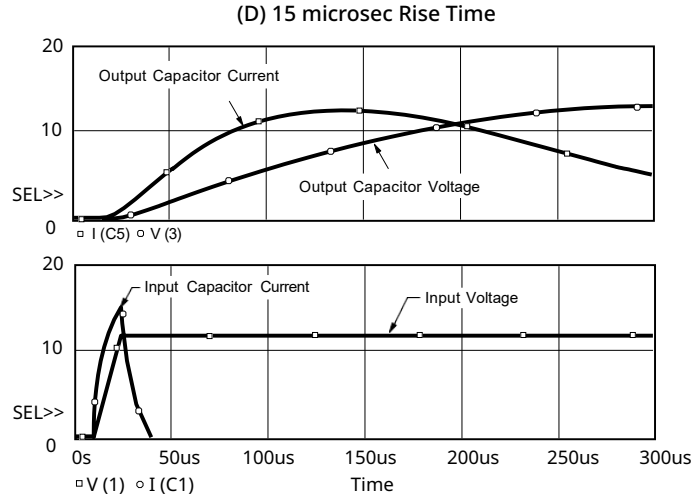

Figure 5 - 15 Microsecond

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The 20 microsecond plot: $I_{MAX} \cong 12$ amps

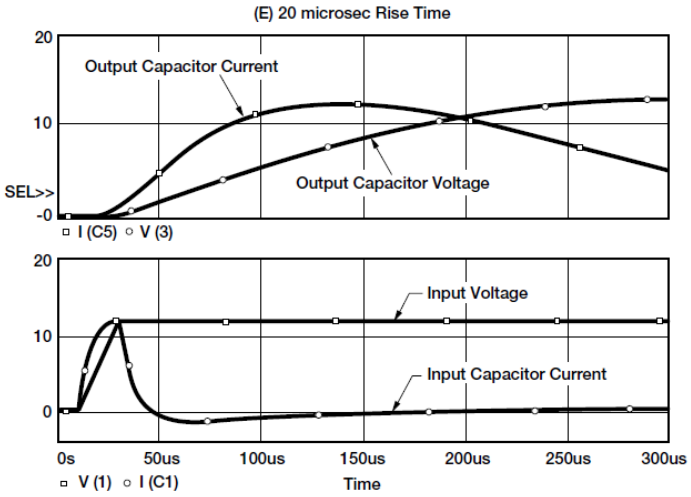

Figure 6 - 20 Microsecond

The 30 microsecond plot: $I_{MAX} \cong 8$ amps

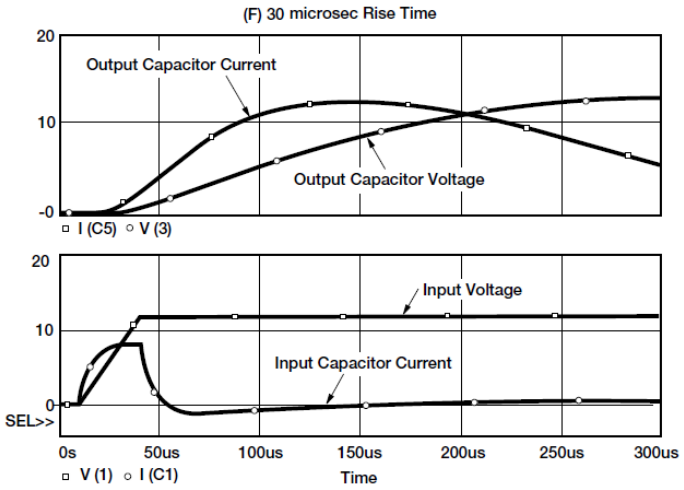

Figure 7 - 30 Microsecond

The amount of surge current a component can handle depends on its rated voltage. The thicker the dielectric the more current it can handle. This is another reason why increased voltage derating will increase the reliability of the circuit design. The following table indicates surge current test failure results of different voltage components. The current was kept constant with the dielectric thickness used as the variable in the experiment. The relationship of the tantalum pentoxide dielectric thickness to forming voltage is 17 angstroms performing volt.

Capacitor Working Voltage (V)	16	16	16	20
Formulation Ratio	3.4 : 1	3.8 : 1	4.1 : 1	4.3 : 1
Formulation Voltage (V)	54.4	61.2	65.7	87.1
Dielectric Thickness (nm)	**92.5**	**104.0**	**111.7**	**148.1**
12V Current Limit = 3A	0.4%	0.2%	0%	0%
12V Current Limit = 5A	0.4%	0.2%	0%	0%
16V Current Limit = 3A	6.8%	6.6%	2.4%	0.2%

Table 1 - Dielectric thickness against surge

There is another potential failure mechanism produced by the resonance that can be developed in the capacitor itself when subjected to a high dv/dt. This resonance will not be discussed in depth in this paper. That resonance consists of the leadframe inductance, anode riser wire inductance, ESR and capacitance of the capacitor. According to reported studies, this resonance can produce a higher voltage across the capacitor than the applied. This phenomena is reported to exist on higher voltage rated parts rather than the lower voltage ones. This is due to the energy storage function of $cv^2/2$ where the voltage exponentially affects the energy stored in the capacitor. Overshoots of an average 20 volts were reported on 50 volt rated capacitors in the experiments.[8]

We have looked at two separate scenarios that can produce failures in tantalum capacitors. One dealing with a high current in-rush due to low impedance in the circuit, the second with a high dv/dt in a reactive circuit. Both examples can be prevented by the control of the voltage rise/fall time in the circuit.

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How to Prevent Current In Rush

The current recommendation for impedance in power circuit applications with dynamic conditions (i.e. voltage and current transients) is one ohm per working volt. This is the standard recommendation for dynamic state conditions. The addition of resistance in the circuit assist in two ways. First, it provides damping resistance for decreasing the Q of the circuit. Second, it reduces the magnitude of the current in-rush.

For example, if you are using a 22 microfarad capacitor rated at 25 volts on a 12 volt power supply rail you would need 12 ohms of impedance to maintain the established reliability level for steady state conditions. However, this is not a practical solution as it defeats the objective of the filtering application.

With the increasing availability of P-Channel Enhancement MOSFETs within the electronics industry, a more realistic solution is possible. This solution adds an integration circuit prior to the capacitor to allow a slow ramp of current into the circuit.

P-Channel Enhancement MOSFET

It is still true that N-Channel MOSFETs have lower $R_{(DS)ON}$ than P-Channel MOSFETs for the same size of die, but the drive within the electronics industry to operate MOSFETs at lower voltages has produced fourth generation low-threshold voltage P- and N-channel vertical diffused MOSFETs. Manufacturers can now produce P-DMOSFETs with typical on-resistance of 40 mohms. The P-Channel MOSFET eliminates the need of level shifting bias that traditional N-Channel MOSFETs required for controlling switch on. This provides the engineer an elegant solution for controlling current in-rush. Component count and circuit cost is reduced by using P-Channel MOSFETs rather than N-channel.

This low $R_{(DS)ON}$ is possible by increasing the number of MOS transistors used in parallel within the die area. The fundamental principle is the same for any MOS technology, increase the cell density to decrease the $R_{(DS)ON}$. Tradeoffs do exist when this is accomplished. Typically thinner oxide levels are used which decreases the maximum gate to source voltage. The thinner oxides do allow for higher transconductance (g_M) and lower $R_{(DS)ON}$ of the FET channel. Similar tradeoffs are made when a tantalum capacitor is selected. Typically selecting a higher voltage component will decrease the allowable capacitance in the same size package.

Planar DMOS structure allows cell densities in excess of 6.7 million/in^2 for Siliconix's (DMOSFET) technology.[9] Vertical power structures were coupled with VLSI techniques to increase cell densities for Motorola's HDTMOS technology.[10] National Semiconductor, Texas Instruments, and several other major silicon manufacturers are developing their own technology to produce more efficient MOSFETs. With this allocation of resources within the industry, the use of P-Channel MOSFETs becomes cost feasible and availability less of a concern.

Figure 8 illustrates the use of a P-Channel MOSFET used in controlling switch on of a 7.5 volt source.

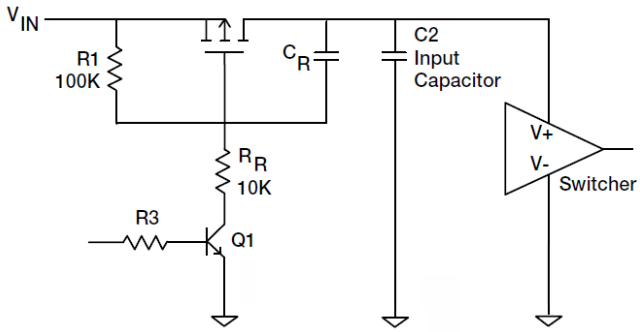

Figure 8 - PFET Integration Circuit I

Using Q1 as the control switch, when a positive voltage is applied the P-Channel MOSFETs gate voltage (V_G) will head toward 0 volts with a time constant of C_R x R_R. Once the MOSFET starts to turn on, the V_G will hold around V_{IN} - 2 volts while the integrator continues to charge. Care must be taken in selection of the voltage divider and PN drop of the transistor to ensure the threshold for turn on of the gate is not exceeded.

The current through R_R and C_R is approximately:

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(V_{IN} - 2) / R_R. The MOSFET will then cause the V_{out} to ramp at a rate of:

$$I = C_R \, dv/dt$$

Substituting (V_{IN} - 2) / R_R) for I and rearranging:

$$((V_{IN} - 2) / R_R) \bullet 1/C_R = dv/dt$$

$$(V_{IN} - 2) / (R_R \, C_R) = dv/dt$$

The ramp rate of the Input Capacitors is the same as the ramp rate of V_{out}. The current into the Input Capacitors is:

$$I_{Input\ Capacitors} = C_{Input} \bullet dv/dt = C_{Input} \bullet (V_{IN} - 2\ v) / (R_R \, C_R)$$

Substituting C_{Input} = 150.0 µf
V_{IN} = 7.5 v
R_R = 10 kohms
C_R = 0.1 µf

dv/dt = (7.5v - 2.0v) / (10 K • 0.1 µf)
= 5.5 kv/s = 5.5 v/ms

Using 150 µf for our input capacitors produces a peak current of:

$$I_{Peak} = 150\ \mu f \bullet 5.5\ v / ms = 0.825\ amps$$

We can use the same approach to simulate the original recommendation of three ohms per working volt that researchers found was the maximum allowable current to allow self healing of the tantalum capacitor's dielectric. Using 0.33 amps as our maximum allowable current, and the same value input capacitor as in our previous example we have:

$$I_{Input\ Capacitors} = C_{Input} \bullet dv/dt = C_{Input} \bullet (V_{IN} - 2\ v) / (R_R \, C_R)$$

Substituting C_{Input} = 150.0 f
V_{IN} = 7.5 v
$I_{Input\ Capacitors}$ = 0.33 amps
R_R = 10 Kohms
R_1 = 100 Kohms

Yields:

$R_R \, C_R$ = (150 µf / 0.33) (5.5)
C_R = 0.25 µf

We will substitute a standard capacitor value of 0.22 µf for completion of this example.

dv/dt = (7.5v - 2.0v) / (10K • 0.22 µf) = 2.5 kv / s
= 2.5 v / ms

$$I_{Peak} = 150\ \mu f \bullet 2.5\ v / ms = 0.375\ amps$$

This provides the maximum theoretical reliability according to original industry research for the majority of capacitors.[3] The variables of dielectric purity, magnitude of manufacturing stresses, and vendor differences (variations) in screening and manufacturing are reduced in their influence on overall reliability when the current in-rush is controlled to this low level of stress exposure. The voltage derating rules of 50% should still be adhered to for component selection in the above recommendations. Once again, reliability will increase with derating.

An alternative circuit configuration that eliminates the variability of the gate threshold level is shown in Figure 9. The integration circuit of R4 and C1 allows the base of the NPN transistor to ramp the collector voltage to the MOSFET gate at a calculated rate.

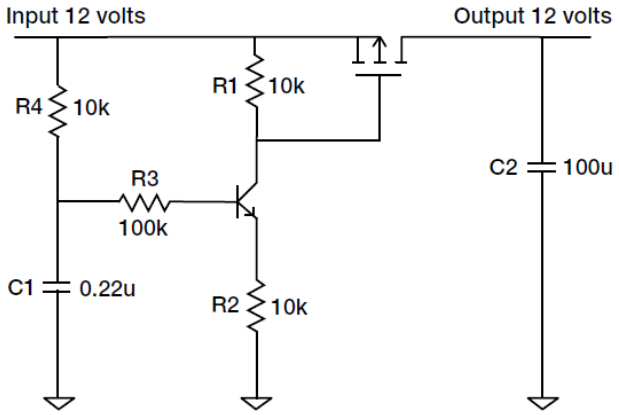

Figure 9 - PFET Integration Circuit II

Figure 10 shows the resultant waveforms for the voltage across the capacitor and the MOSFET gate voltage. With this circuit, low V_G is required for lower $R_{(DS)ON}$ of the FET. Lower input voltages may not drive the FET into the desired range of operation.

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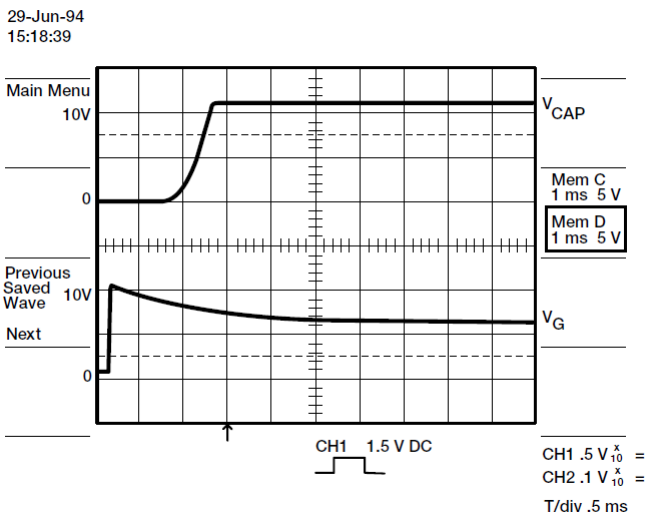

Figure 10 - Voltage Profile

Figure 11 indicates the maximum current from this circuit to be about 1.3 amps. Note that the voltage rise across the capacitor is almost linear. The resultant maximum current of approximately 1.3 amps for a 0.9 millisecond rise time is confirmed mathematically through the expression i = c • dv/dt

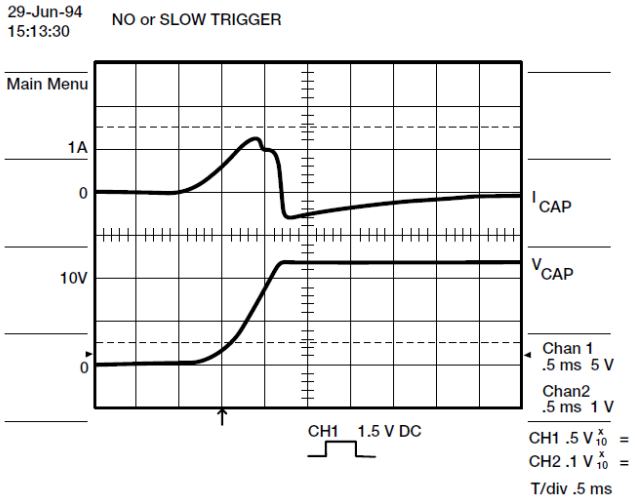

Figure 11 - Voltage and Current Profile

Figure 12 is the gate voltage of the MOSFET as it turns on.

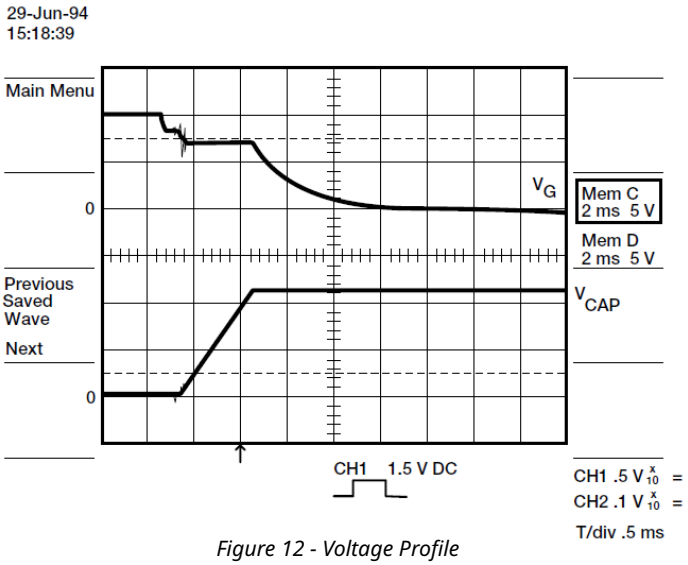

Figure 12 - Voltage Profile

One more circuit configuration worth exploring utilizes the capacitor on the source side rather than the drain. Figure 13 shows this configuration. R_C is required to ensure C_R and gate capacitance are discharged at turn on. The MOSFET starts to turn on at V_T (Voltage Threshold). Therefore there is a time delay before any current will pass on to C_T.

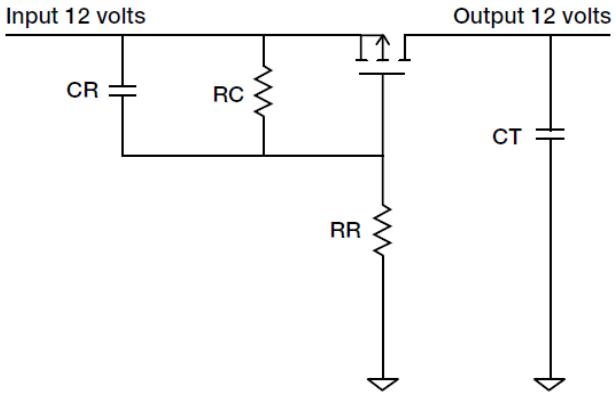

Figure 13 - PFET Integration Circuit III

$$t_1 = - R_R C_R \ln (1 - V_T / (V_{SS} - V_{G_{MAX}})$$

where $V_{G_{MAX}} = (R_R / R_R + R_C) \times V_{SS}$

This equation is derived from

$$V_G = (V_{SS} - V_{G_{MAX}}) (1 - e^{-t / (R_R C_R)})$$

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We could substitute $V_{CR_{MAX}}$ in the place of $V_{G_{MAX}}$ where

$$V_{CR_{MAX}} = (R_C / (R_R + R_C)) V_{SS}$$

Assume V_T = 1.5 volts, R_R = 100 kohms, C_R = 470 nF, V_{SS} = 12 volts, R_C = 100 kohms

$V_{CR_{MAX}}$ = 100 kohms / (100 kohms + 100 kohms) (12)
= 6 volts

t_1 = (-100 K) (470 n) (ln (1 - (1.5/6)))
= 13.52 mS

V_G will fall as C_R charges and the MOSFET will enter the saturation region at around 3 to 4 volts applied across V_{GS}. At this time the tantalum capacitor will be fully charged.

$$t_2 = -R_R C_R \ln (1 - (V_{SAT} / V_{CR_{MAX}}))$$

Assume V_{SAT} = 3 volts

t_2 = 32.58 ms

The rise time, t_1, for V_{CT} is therefore 32.58 - 13.52 = 19.06 ms.

Maximum current is I = C dv/dt

$= C_T \times V_{SS} / t_r$:Assume C_T = 100 µF
$= 100\ \mu \times 12 / 19.06 \times 10^{-3}$
= 0.063 amps

To calculate C_R from peak current required, first set R_C and R_R. For our example R_C = 100 kohms and R_R = 10 kohms.

$V_{CR_{max}}$ = (100 k / (100 k + 10 k))(VSS)
= 10.9 volts

I = $C_T \times V_{SS} / t_r$: We want 1 amp for our example

t_r = 100 µ x 12 / t_r
= 1.2 ms
= - R_R C_R [ln (1 - V_{SAT} / $V_{CR_{MAX}}$)
- ln (1 - V_T / $V_{CR_{MAX}}$)]

The second part of the equation, ln (1-V_{SAT} / $V_{CR_{MAX}}$) - ln (1-V_T / $V_{CR_{MAX}}$), represents a constant for each MOSFET type, in this case -0.174 volts.

t_r = 0.174 R_R C_R
1.2 m = 0.174 x 10 k C_R
C_R = 689 nF

The nearest standard value is 680 nF.

Adding an NPN transistor as shown in Figure 14 can provide an on / off signal for the board power supply.

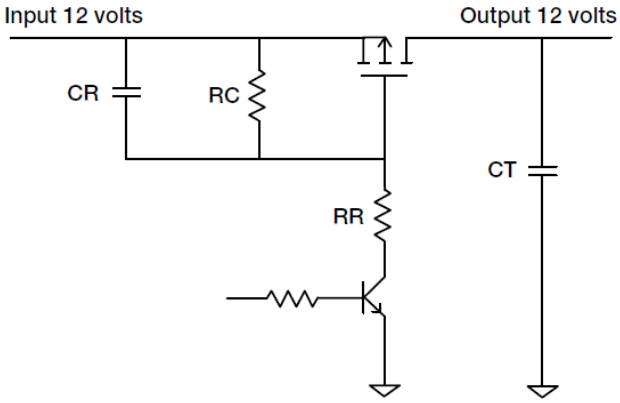

Figure 14 - PFET Integration Circuit III with Switch

Hence, by utilizing the P-Channel MOSFET as a switch controlled by a simple integration circuit we are able to effectively reduce current in-rush by eliminating the step function response. A list of several manufacturers of low R_{ON} MOSFETs are provided in the summary. New models and product lines are being added regularly so check with your manufacturer of choice for updates. At the time of this publication, these P-Channel MOSFETs were relatively inexpensively priced for the increase in tantalum capacitor reliability provided.

Another option for controlling the dv/dt of the input voltage is the use of high side MOSFET drivers. These devices are manufactured by several different vendors, but our discussions here will focus on the Linear Technology LTC115X family. These MOSFETs require no , or little if any, external components for usage. Each device uses low $R_{DS(on)}$ N-Channel MOSFET switches.

The obvious problem of level shifting to produce the gate voltages higher than the power supply voltage is overcome by the use of built in charge

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pumps to fully enhance the switches. The devices come in single, dual, and quad packages. General voltage range for operation is from 2.7 to 18 volts depending on the device in the family selected.

These devices are intended to prevent the power supply lines from glitching during turn on by controlling the dv/dt. Figure 15 shows a LTC1154 used to control the turning on of a 5 volt supply rail. In this example an integration circuit using a 100 kohm resistor and a 0.33 microfarad capacitor controls the slew rate of the MOSFET gate to approximately 1.5 x 10^{-4} v/µs. This works out to be about 15 milliamps of start up current.

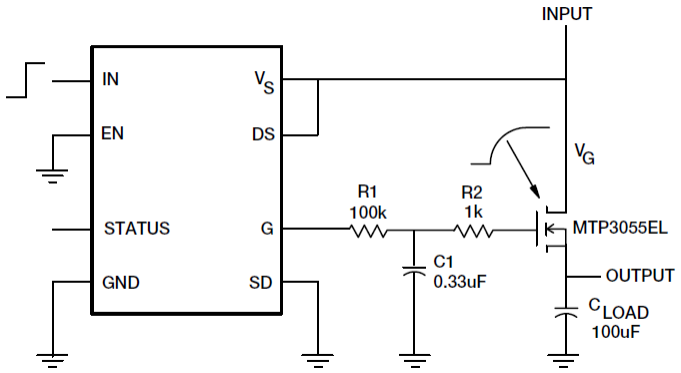

Figure 15

CONCLUSION

In summary, the magnitude of current in-rush a component will receive is controlled in a large part by its inherent ESR in low impedance applications. Capacitors which have low ESR can be subjected to higher stress levels than higher ESR components. Circuit application failures of tantalum capacitors can fall into two categories, high dv/dt or high current in-rush. Controlling the dv/dt of the circuit will increase the reliability of tantalums in low impedance applications for both cases. New generation P-Channel MOSFETs can be a cost effective solution for reducing current in-rush failures of tantalum capacitors.

REFERENCES

1. Hasegawa, Y., "A Study of Field Failures of Solid Tantalum Capacitors", NEC Research and Development (July, 1986)
2. Souza, E., "Testing of Solid Tantalum Capacitors - Low Impedance, High Inrush Currents", Mepco-Electra (December, 1983)
3. Mogilevsky, B. and Shirn, G., "Surge Current Failure in Solid Electrolyte Tantalum Capacitors", IEEE Transactions On Components, Hybrids and Manufacturing Technology (December, 1986)
4. Holladay, Dr. A. M. and Moynihan, J., "Effectiveness of Surge Current Screening of Solid Tantalum Capacitors", Sprague TP83-2
5. Gill, J., "Surge in Solid Tantalum Capacitors", AVX (July, 1994)
6. "TPS Low ESR SM Tantalum Capacitor Catalog", AVX (1993)
7. Hageman, S., "Simple PSpice Models Let You Simulate Common Battery Types", EDN (October 28, 1993)
8. Holland, H., "Effects of High Current Transients on Solid Tantalum Capacitors", Kemet (1976)
9. Goodenough, F, "P-DMOSFET and TSSOP Turns on with 2.7 VGS", Electronic Design (May 2, 1994)
10. Deuty, S., "Synchronous Rectifiers Boost Efficiency", Electronic Engineering Times (May 23, 1994)
11. Lutz and Makowski, Testing with High Frequency Transients, Test and Measurement (February 1992)
12. Gill, J., "Basic Tantalum Technology", AVX (1994)

COMPONENT SOURCES

1. Texas Instruments	TPS1101	$r_{DS(on)}$=0.090 ohms
	TPS1100	$r_{DS(on)}$=0.180 ohms
2. Motorola	MMSF4P01HD	$r_{DS(on)}$=0.080ohms
	MTD20P03HDL	$r_{DS(on)}$=0.090 ohms
	MTP23P06	$r_{DS(on)}$=0.120 ohms
	MTP50P03HDL	$r_{DS(on)}$=0.030 ohms
3. Siliconix	Si9435DY	$r_{DS(on)}$=0.090 ohms
	Si9430DY	$r_{DS(on)}$=0.080 ohms
4. International Rectifier	IRF7204	$r_{DS(on)}$=0.060 ohms

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